Proposal for Digitizer-to-SLINK Interface Card

J. Pilcher
(for Haifeng Wu)

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Overview

- Located in drawers (1 interface board/drawer)
- Input from 8 digitizer boards (16 DMU chips)
- Output to ROD modules via SLINK
Goals for new design

- No timing adjustments needed from digitizer boards
  - Easy setup and reliable long-term operation
- Complete 2-fold redundancy to RODs
  - Reviewers questioned single point of failure in drawer interface
- Data formatted in 32-bit words from one DMU at a time (“natural format”)
  - Transparent format for easier debugging & easier spotting of failures
Goals for new design (cont.)

- Can order sequence of output channels according to drawer geometry, or tower geometry
  - Simplifies interface with ROD
- SLINK/GLINK interface built into board
  - No mezzanine card
  - Much more compact
  - 640 Mb/s capability (standard)
  - 346 Mb/s required for TileCal (@75 MHz LVL1A rate)
    - Derandomizing buffers on digitizer boards
Goals for new design (cont.)

- Use no custom chips
  - Avoid high development costs and long delays
  - Programmable commercial devices
    ▲ EPLD or FPGA like Altera, Xilinx, Actel
    ▲ Studies so far with Altera 20K100 (100K gates, 3ns gate delay)
Organization

- Dual structure of interface card for redundancy
  - All complexity in “Interface Logic” chips

Figure 2: Block diagram of interface board.
Organization

- Serial-to-parallel (SP) input stage for each DMU
  - Individual data clocks from each digitizer board
- Data time-aligned by Pipe
- Data accumulated in Input Buffer (2 page buffer)
- Data delivered to Output FIFO in desired order

Figure 3: Block diagram of the interface logic chip
Serial-to-Parallel Converter

- Pair of bits from serial inputs every 25 ns
- 32-bit output every 400 ns
- SP converters asynchronous in pairs (8 input clocks)

Diagram:

- Logic controller
- 16 bit shift register
- Preset
- Comparer
- Format 32 bitwords (according to protocol)

Note: every two SP converter share one group (wen_in, ctrl_in, clock_in) signals from one digitizer board, mean while each of them own two data inputs from different DMU of the digitizer board.
Pipe Section

- 32-bit input registers loaded asynchronously
- Unloaded one register every 50 ns (8 in 400 ns)
- Input registers free after 200 ns (4 double-buffers)
Master Clock Section

- Choose one out of 3 possible clocks at reset time
- Each interface logic chip has one of these (redundant)

During reset circle the logic controller enables 3 counters, and compare the counts, it picks the clock that equals or only has 1 count different from one of other two. The default clock is clock1.
Status

- Most VHDL code written and tested
- Must fully simulate timing margins

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Planning

- Requesting concept approval by TileCal
- Submit proposal for funding to US ATLAS
  - Additional source of funding for readout
  - Action in 6 months?
- Continue design and prototyping
  - Details to be agreed to with Stockholm
  - Clearly written interface specifications needed
- System demonstration test with prototype within 1 year
  - Production would follow

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