

CYCLONE IV E CONFIGURATION SETTINGS

CONF	SCHM	MSEL2	MSEL1	MSEL0	CONF	VOLT
1	0	1	FAST	3.3		
1	0	0	FAST	3.0	2.5	
0	1	0	STD	3.3		
0	1	1	STD	3.0	2.5	

SCH#: B-2892
SPC#: B-2893
ASM#: B-2894

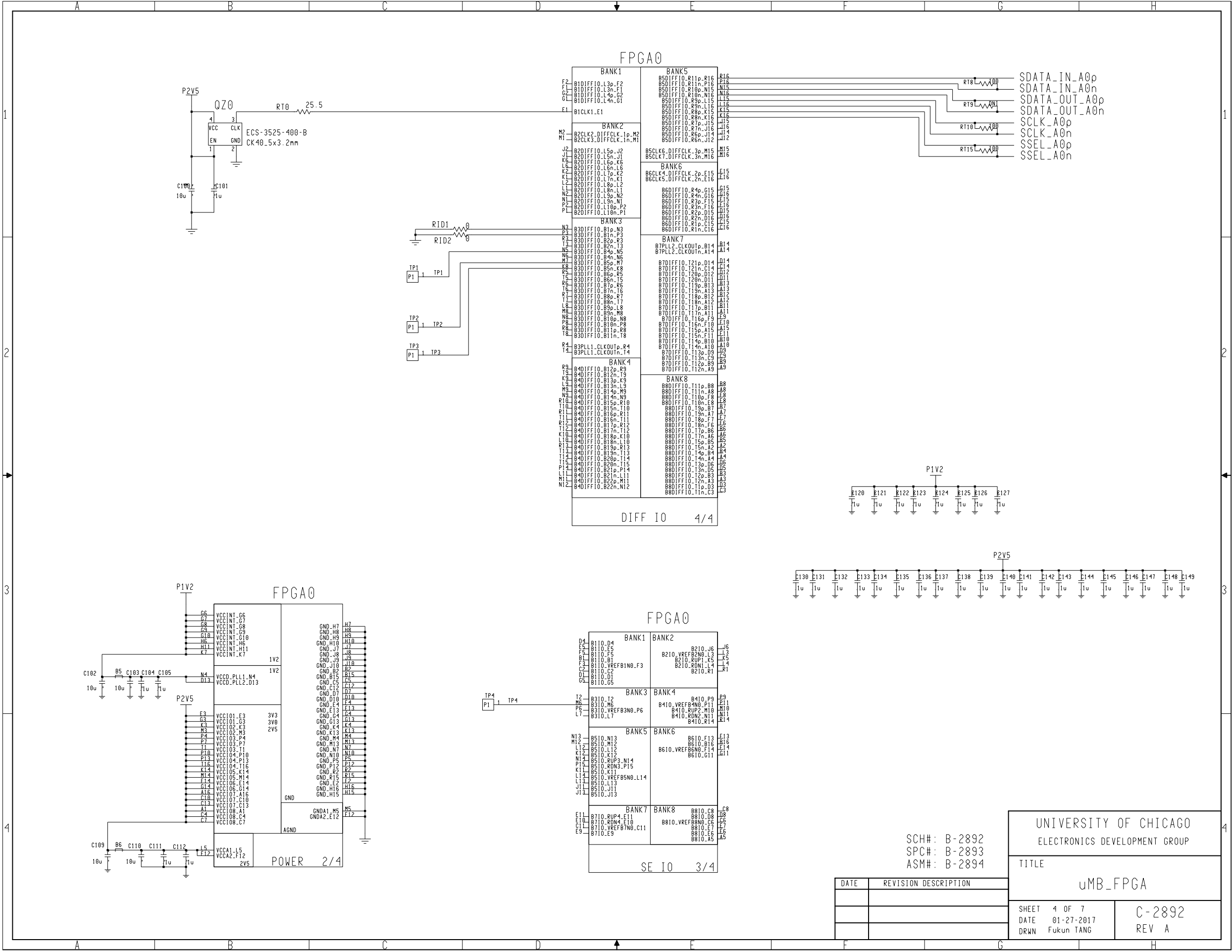
DATE	REVISION	DESCRIPTION

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
FPGA CONFIG CHAIN1

SHEET 2 OF 7
DATE 01-28-2017
DRWN Fukun TANG

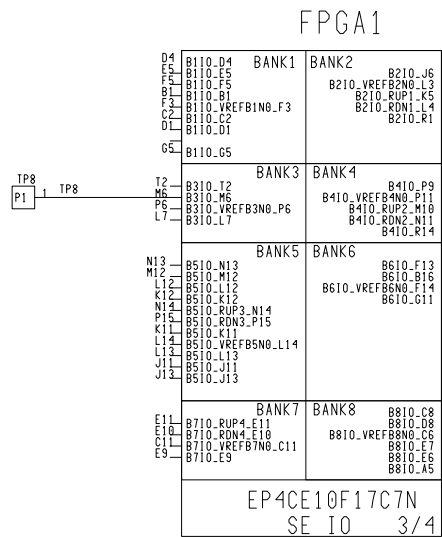
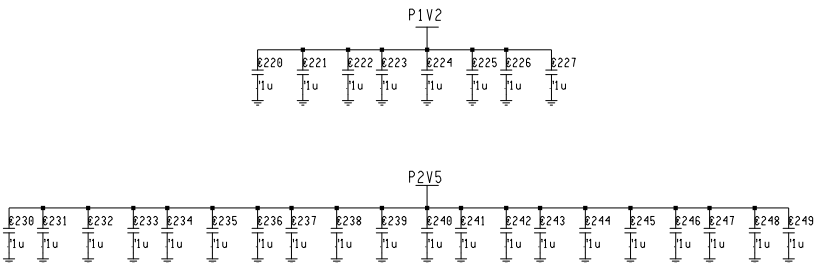
C-2892
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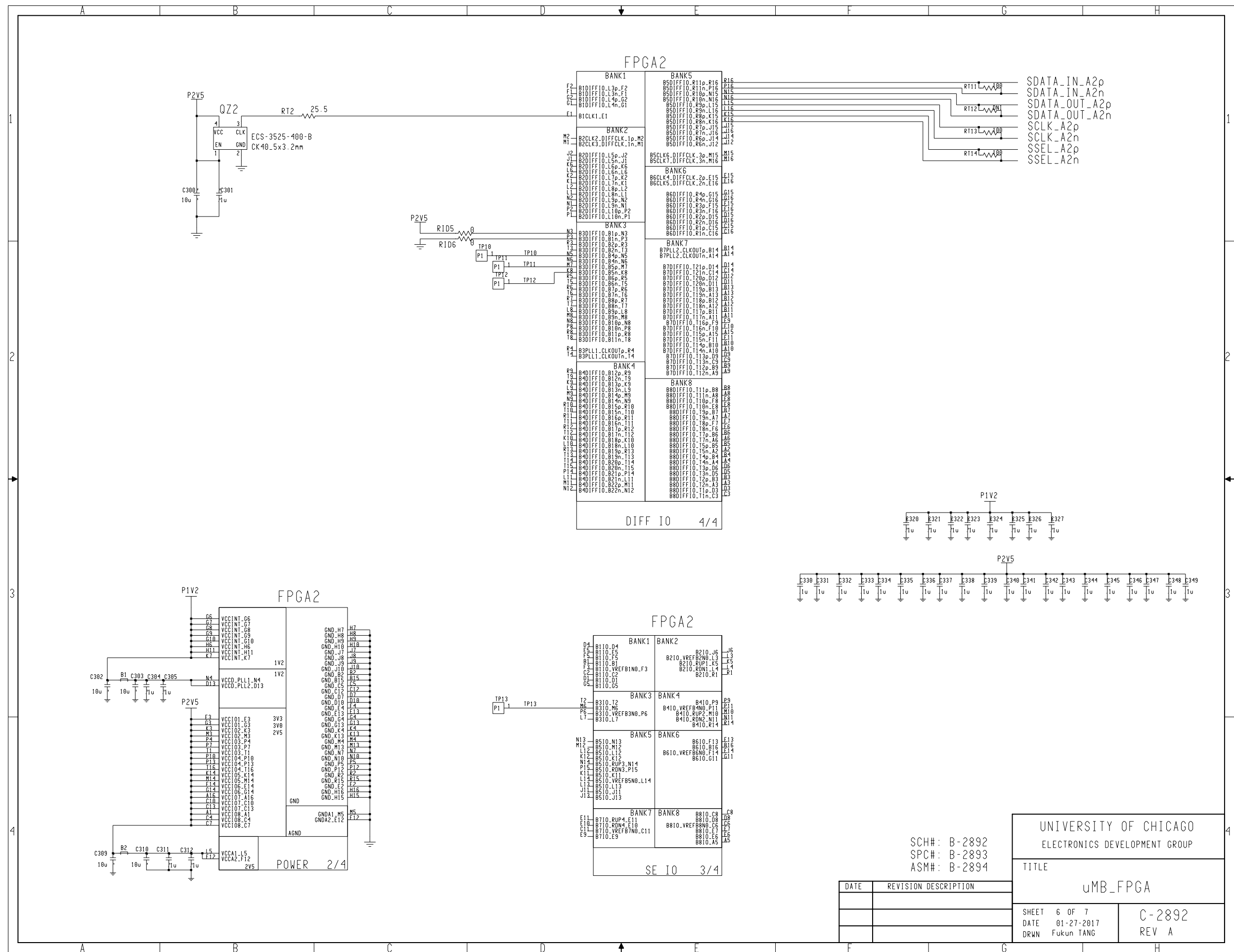
SCH#: B-2892
SPC#: B-2893
ASM#: B-2894

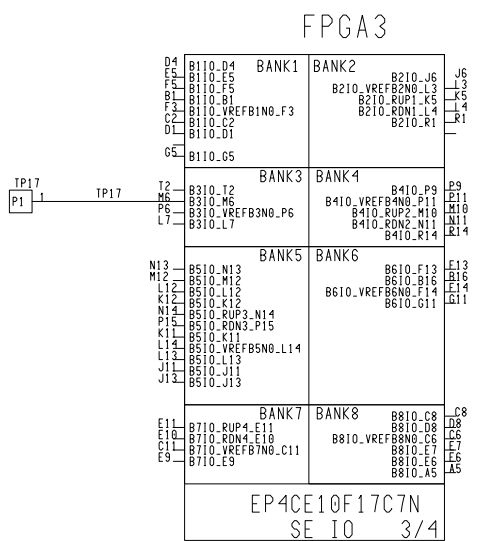
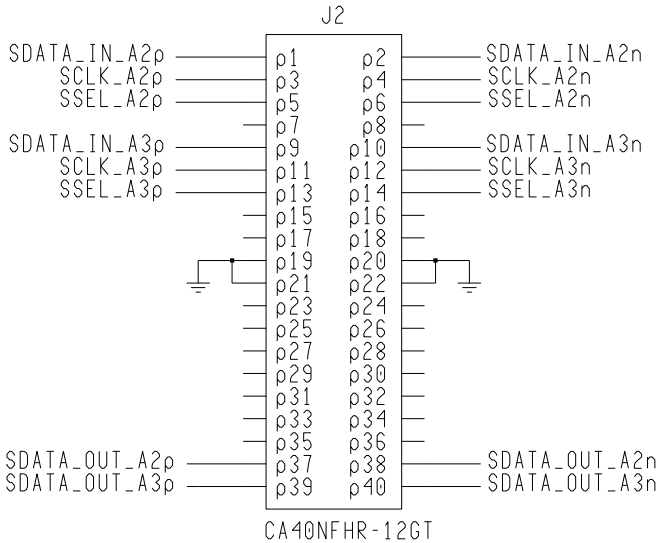
DATE	REVISION DESCRIPTION

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SHEET 4 OF 7 DATE 01-27-2017 DRWN Fukun TANG	C-2892 REV A



SCH#: B-2892		UNIVERSITY OF CHICAGO	
SPC#: B-2893		ELECTRONICS DEVELOPMENT GROUP	
ASM#: B-2894		TITLE	
		uMB_FPGA	
DATE	REVISION DESCRIPTION		
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		DATE 10-21-2016	
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SPC#: B-2893		
ASM#: B-2894		
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		SHEET 7 OF 7
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