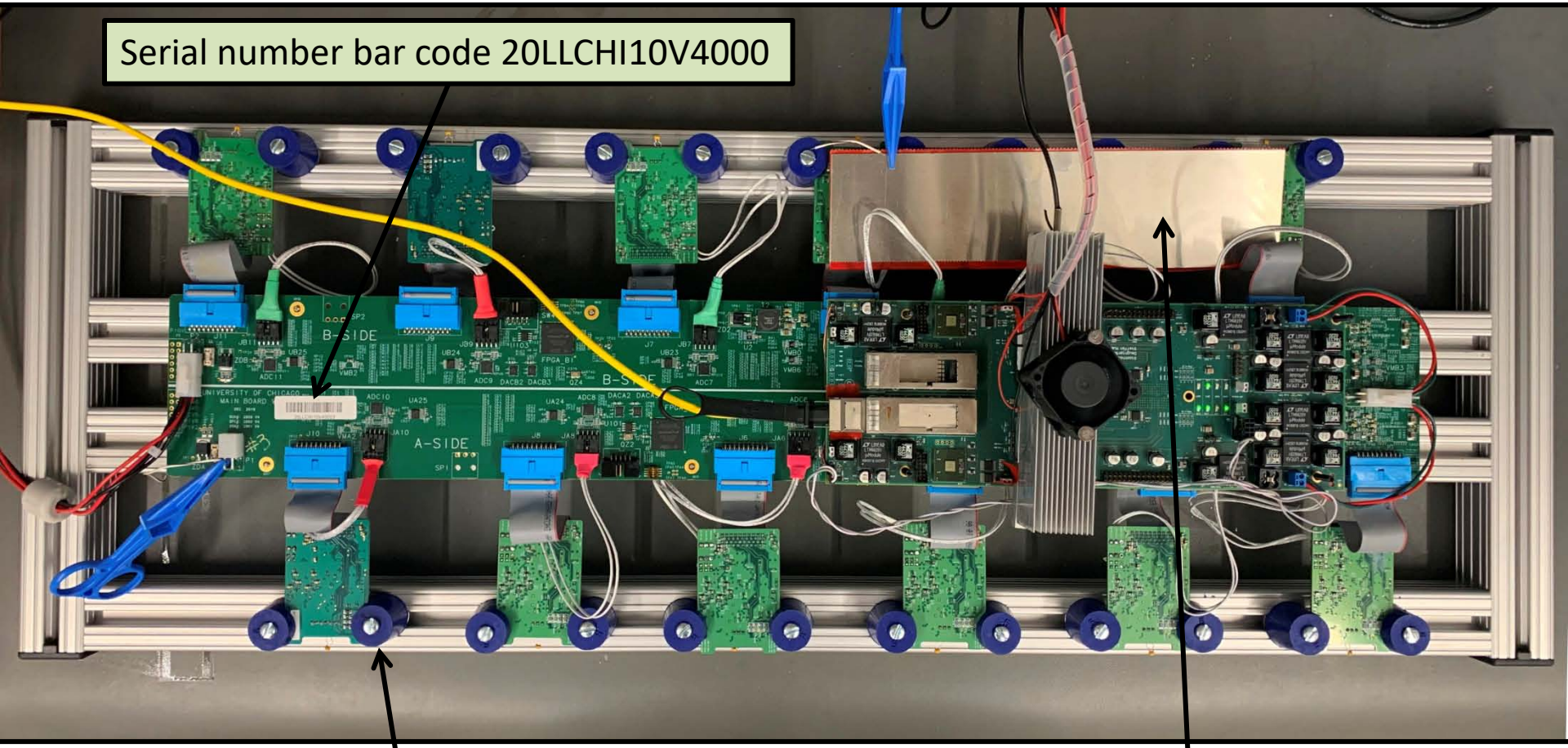
Test Stand

It looks a lot like the Clermont Ferrand test stand since I copied their setup.

We plan to have 4 test stands with DBv6s



After Burn-In is completed, we need to do final test of all of the functions of the mainboards before sending them to CERN or other labs.

Step 1

For burn-in, special firmware is used for the FPGAs that uses the onboard 40MHz clock.

========== load physics firmware ==========

Step 2

Test the DB to PPR (or Emulator) connection is good

======== run ResetLinksv5.py (Alberto's code) ==========

```
-bash-4.2$ python ResetLinksv5.py -m 1 -c A0 -d RX -b DB -g A
communicating with host
communication successful
 Resetting wait 1 second...

 Resetting FPGA A wait 1 second...

 ==========================================================================================================================
------ TX_PLL - RX_FRAMECLK - RX_WORDCLK - MGT_RDY - BITSLIPNb  - GBTRX_RDY - GBTTX_RDY_LOST - DATA_ERROR -
SideA0: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideA1: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideB0: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideB1: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
 ==========================================================================================================================
------ TX_PLL - RX_FRAMECLK - RX_WORDCLK - MGT_RDY - BITSLIPNb  - GBTRX_RDY - GBTTX_RDY_LOST - DATA_ERROR -
SideA0: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideA1: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideB0: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideB1: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
 ==========================================================================================================================
------ TX_PLL - RX_FRAMECLK - RX_WORDCLK - MGT_RDY - BITSLIPNb  - GBTRX_RDY - GBTTX_RDY_LOST - DATA_ERROR -
SideA0: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideA1: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideB0: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideB1: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
 ==========================================================================================================================
------ TX_PLL - RX_FRAMECLK - RX_WORDCLK - MGT_RDY - BITSLIPNb  - GBTRX_RDY - GBTTX_RDY_LOST - DATA_ERROR -
SideA0: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideA1: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideB0: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideB1: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
 ==========================================================================================================================
------ TX_PLL - RX_FRAMECLK - RX_WORDCLK - MGT_RDY - BITSLIPNb  - GBTRX_RDY - GBTTX_RDY_LOST - DATA_ERROR -
SideA0: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideA1: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideB0: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
SideB1: -  0     -    1     -      1     -     1    -    0      -     1     -       0        -     0
0
------------------------------------------------------------------------------------------------------------------------
   --------------------------    Bit Error Rate measurements. Minidrawer  1          --------------------------
------------------------------------------------------------------------------------------------------------------------
------ Number of frames - CRC Frame Errors - Fraction per million - Bit Error Rate - Effective Errors
SideA0       160541227            0                0               0.000000e+00               0
SideA1       160541227            0                0               0.000000e+00               0
SideB0       160541227            0                0               0.000000e+00               0
SideB1       160541227            0                0               0.000000e+00               0
0
------------------------------------------------------------------------------------------------------------------------
   --------------------------    Bit Error Rate measurements. Minidrawer  1          --------------------------
------------------------------------------------------------------------------------------------------------------------
------ Number of frames - CRC Frame Errors - Fraction per million - Bit Error Rate - Effective Errors
SideA0       160534329            0                0               0.000000e+00               0
SideA1       160534329            0                0               0.000000e+00               0
SideB0       160534329            0                0               0.000000e+00               0
SideB1       160534329            0                0               0.000000e+00               0
0
------------------------------------------------------------------------------------------------------------------------
   --------------------------    Bit Error Rate measurements. Minidrawer  1          --------------------------
------------------------------------------------------------------------------------------------------------------------
------ Number of frames - CRC Frame Errors - Fraction per million - Bit Error Rate - Effective Errors
SideA0       160530424            0                0               0.000000e+00               0
SideA1       160530424            0                0               0.000000e+00               0
SideB0       160530424            0                0               0.000000e+00               0
SideB1       160530424            0                0               0.000000e+00               0
0
------------------------------------------------------------------------------------------------------------------------
   --------------------------    Bit Error Rate measurements. Minidrawer  1          --------------------------
------------------------------------------------------------------------------------------------------------------------
------ Number of frames - CRC Frame Errors - Fraction per million - Bit Error Rate - Effective Errors
SideA0       160528644            0                0               0.000000e+00               0
SideA1       160528644            0                0               0.000000e+00               0
SideB0       160528644            0                0               0.000000e+00               0
SideB1       160528644            0                0               0.000000e+00               0
wait...
```

Step 3 ====== serno.py =========

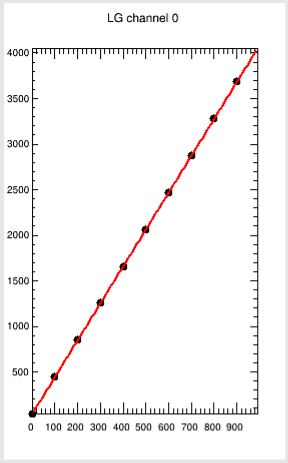
Read the board serial number and make a directory of that name to store test results.

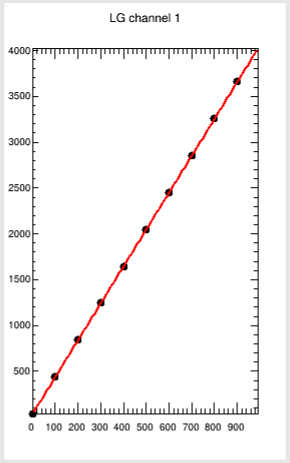
Read/Write to all of the 3in1/FENICS card configuration registers

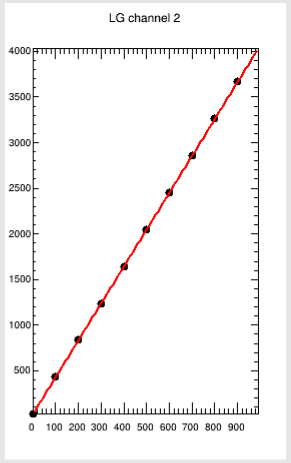
```
-bash-4.2$
-bash-4.2$ python serno.py
communicating with host
communication successful
input MBv4 barcode
20LLCHI10V40003
mkdir: cannot create directory `20LLCHI10V4000': File exists
 =============  card= 0   FPGA= 1   TUBE= 2  ======= 3in1 Latch Bits Toggle ==========
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   0     1     0     1     0     1     0     1
back   0     1     0     1     0     1     0     1
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   1     0     1     0     1     0     1     0
back   1     0     1     0     1     0     1     0
 CHK=  0
 card  0 ===== GOOD =====

 =============  card= 1   FPGA= 3   TUBE= 2  ======= 3in1 Latch Bits Toggle ==========
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   0     1     0     1     0     1     0     1
back   0     1     0     1     0     1     0     1
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   1     0     1     0     1     0     1     0
back   1     0     1     0     1     0     1     0
 CHK=  0
 card  1 ===== GOOD =====

 =============  card= 2   FPGA= 1   TUBE= 1  ======= 3in1 Latch Bits Toggle ==========
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   0     1     0     1     0     1     0     1
back   0     1     0     1     0     1     0     1
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   1     0     1     0     1     0     1     0
back   1     0     1     0     1     0     1     0
 CHK=  0
 card  2 ===== GOOD =====

 =============  card= 3   FPGA= 3   TUBE= 1  ======= 3in1 Latch Bits Toggle ==========
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   0     1     0     1     0     1     0     1
back   0     1     0     1     0     1     0     1
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   1     0     1     0     1     0     1     0
back   1     0     1     0     1     0     1     0
 CHK=  0
 card  3 ===== GOOD =====

 =============  card= 4   FPGA= 1   TUBE= 0  ======= 3in1 Latch Bits Toggle ==========
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   0     1     0     1     0     1     0     1
back   0     1     0     1     0     1     0     1
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   1     0     1     0     1     0     1     0
back   1     0     1     0     1     0     1     0
 CHK=  0
 card  4 ===== GOOD =====

 =============  card= 5   FPGA= 3   TUBE= 0  ======= 3in1 Latch Bits Toggle ==========
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   0     1     0     1     0     1     0     1
back   0     1     0     1     0     1     0     1
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   1     0     1     0     1     0     1     0
back   1     0     1     0     1     0     1     0
 CHK=  0
 card  5 ===== GOOD =====

 =============  card= 6   FPGA= 0   TUBE= 2  ======= 3in1 Latch Bits Toggle ==========
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   0     1     0     1     0     1     0     1
back   0     1     0     1     0     1     0     1
     TPH   TPL   CAL    S1    S2    S3    S4   TRG
sent   1     0     1     0     1     0     1     0
back   1     0     1     0     1     0     1     0
```

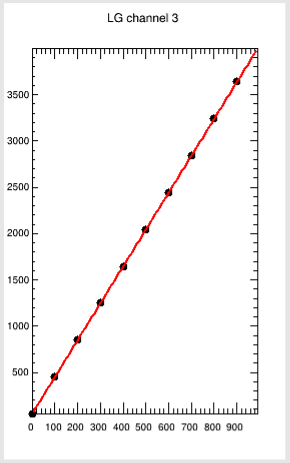
Step 4 ====== offset.py =========

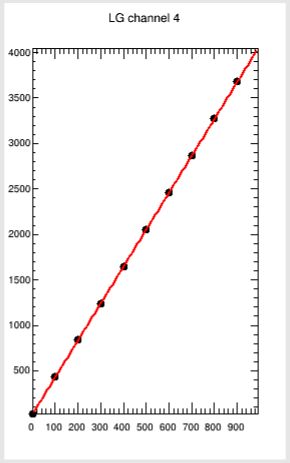
plot the high and low gain offset dac vs ADC Counts

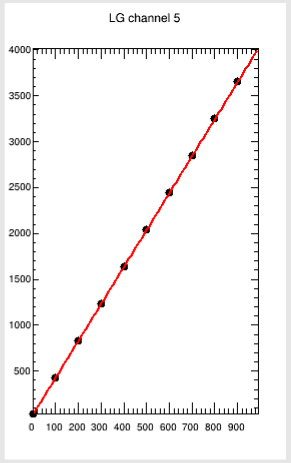


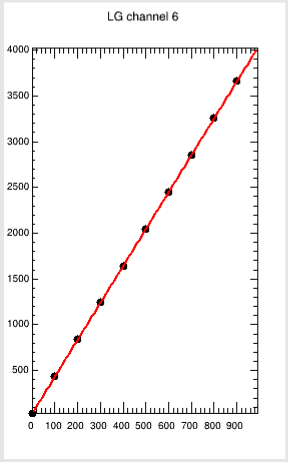


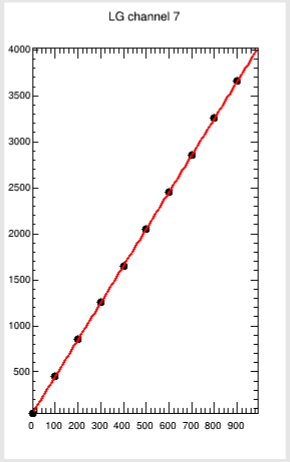


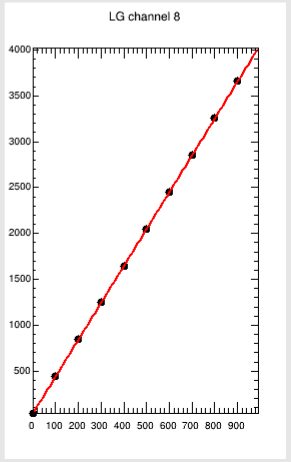


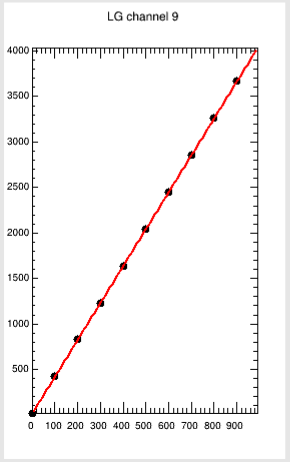


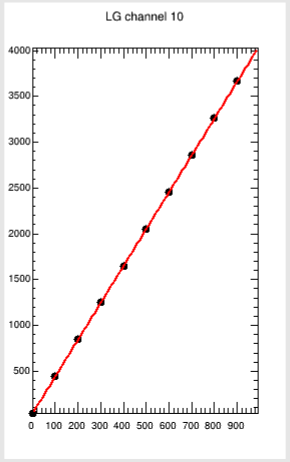


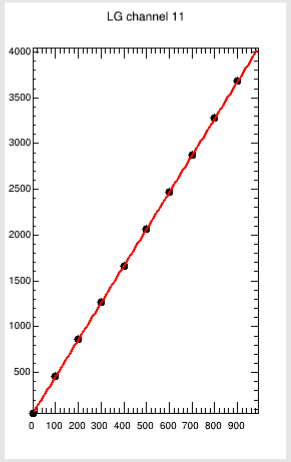






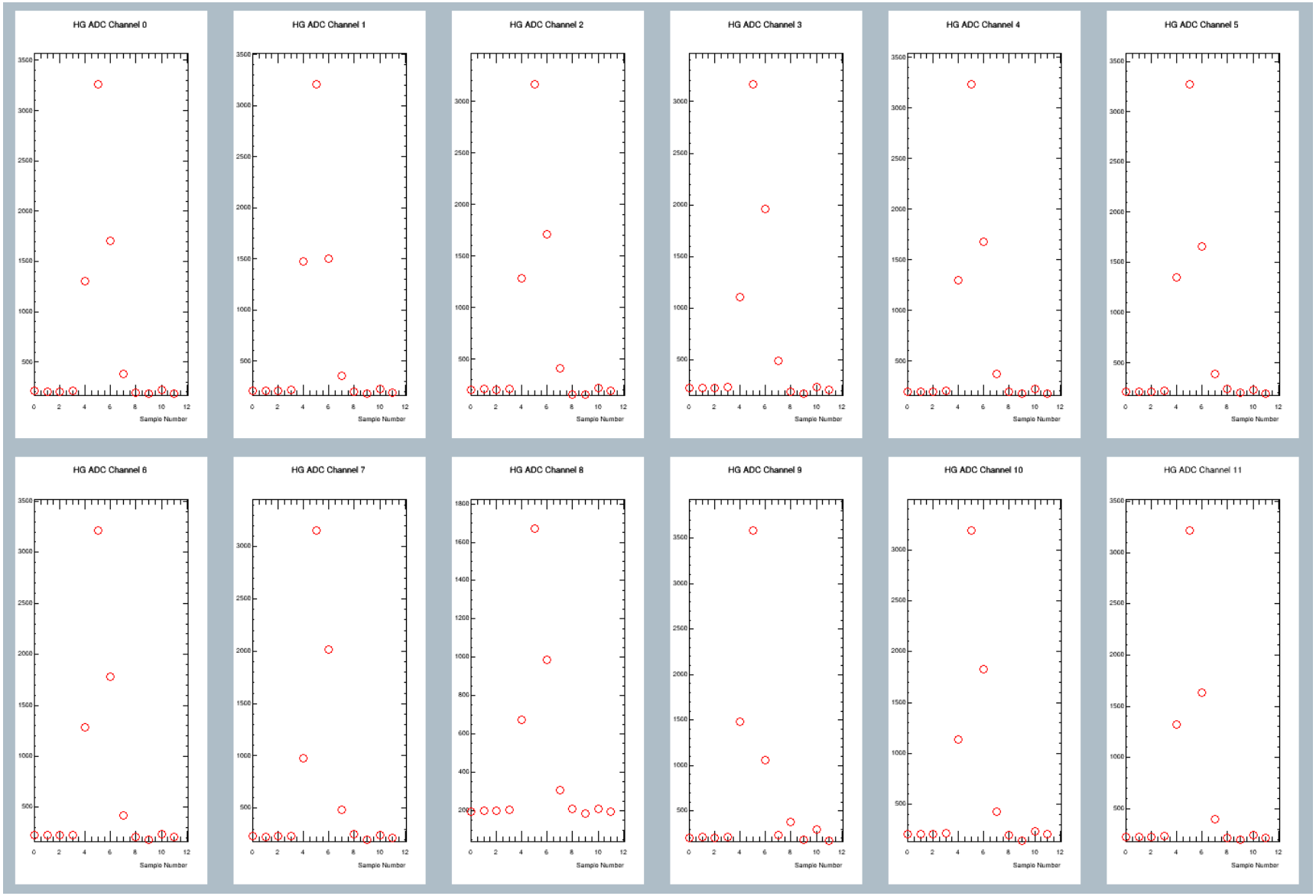






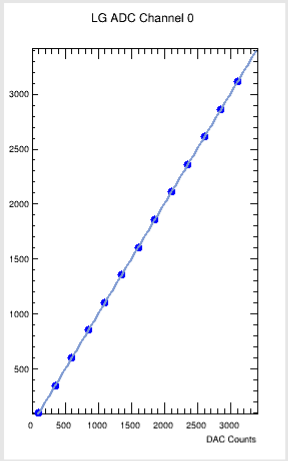
Step 5 ====== evLG.py and evHG.py =========

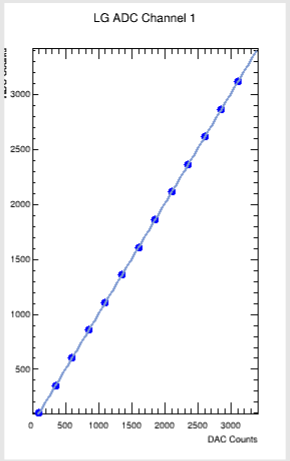
look at pulse shape for each ADC

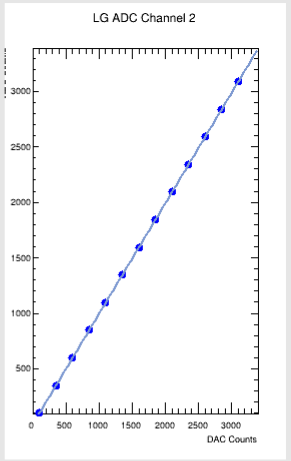


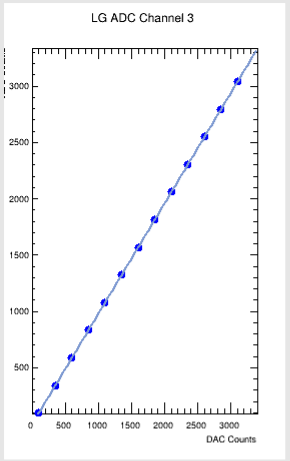
Step 6 ====== cisLG.py and cisHG.py=========

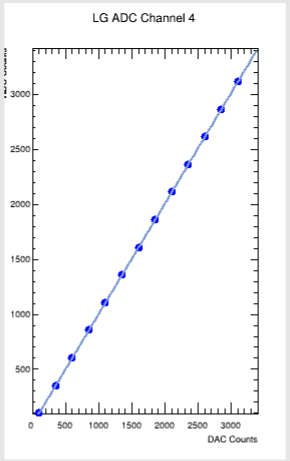
plot the high and low gain charge injections dac vs ADC Counts

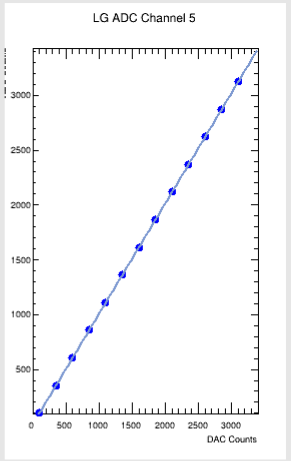


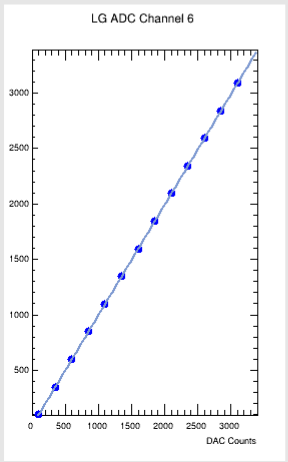


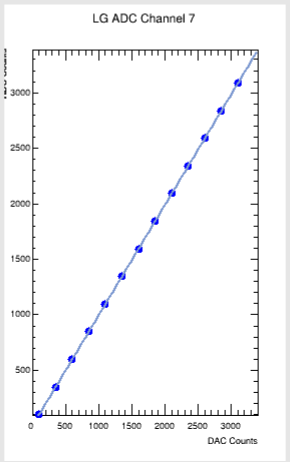


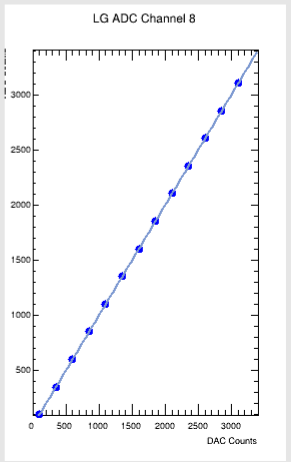


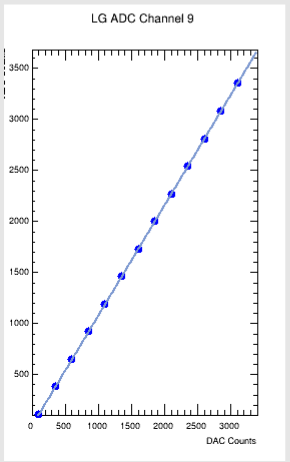


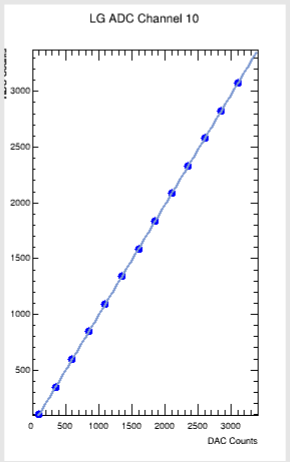


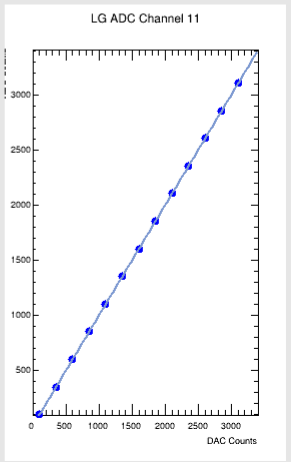








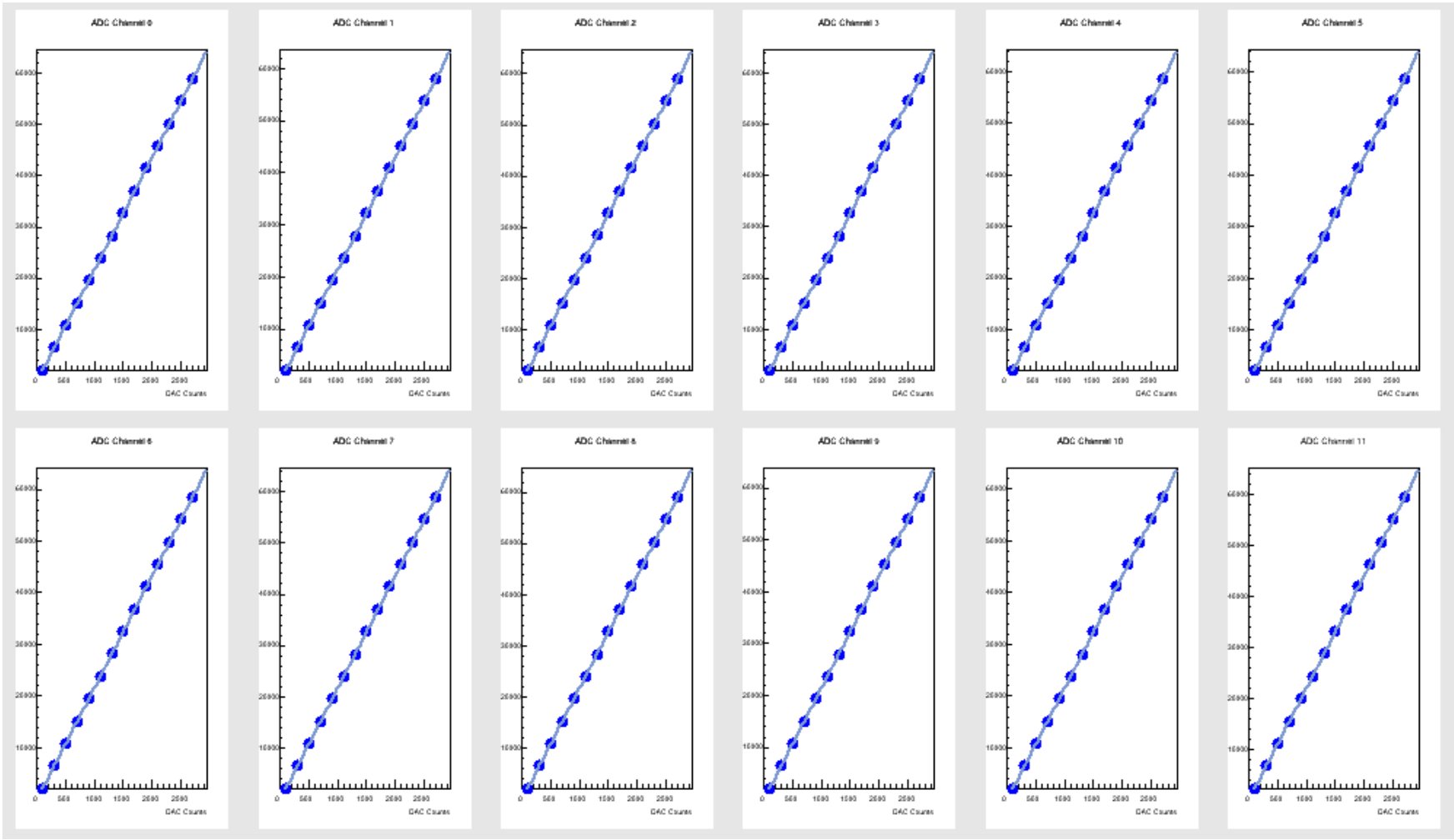




… and other plots RMS vs DAC Fit-Data vs DAC

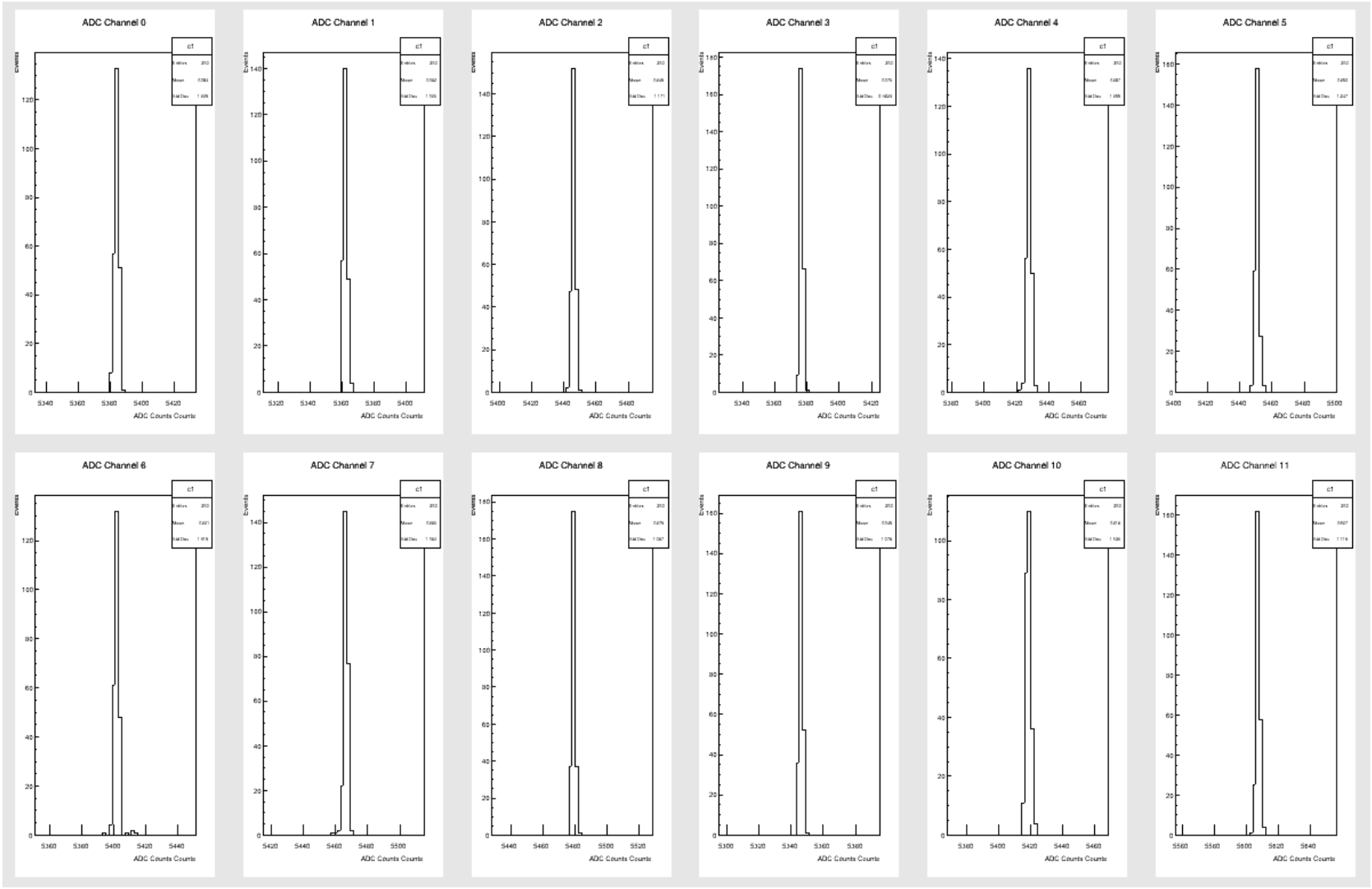
Step 7 ====== intlin.py=========

at lowest 3in1/FENICS gain setting plot DAC vs ADC Counts



Step 7 ====== intres.py=========

plot the resolution at one DAC setting



If all of this looks good, we move on to the next MainBoard.

We need to process each day:

1. remove 4 MainBoards from a Burn-In table.
2. affix serial numbers on 4 new boards
3. program burn-In firmware on the 4 new boards
4. mount then in the heater boxes
5. scan the serial numbers and start the 5 day heat cycle

6. do final testing as outlined above for the 4 boards that came out of the burn-in stand.

…. shipping logistics …. Repairs ….. ?

900 boards …..