Summary

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L2 Pulsar 2nd IRR Review, ICB-2E, video: 82Pulsar

Materials for the review will be available at:
http://hep.uchicago.edu/~thliu/projects/Pulsar/L2_upgrade_meeting.html
Summary

- Preparation work in (the rest of) Feb. 2005
- Readiness for Operation in March. 2005
- Back up slides:
  future system performance optimization
Q&A

- Are we ready for operation?
  - We are getting very close
    - Pulsar system is already robust
    - Pulsar crate running for half year and has been reliable
    - Better performance (than legacy) at high luminosity
    - has been running in auto-reject mode with system since Feb.2 (2005) ➔ Already in “Operation Mode”!

We do have (limited) experience on Pulsar hardware/firmware reliability:
  RunIIa Muon Pulsar has been in the system since Sept, 2003.
  We have never had to touched it and no single error so far.
  No single Pulsar board failure in the past few years (~40 extensively used)
There are still work to do

- Most important action items (the rest of the month):
  - Fully test the new readout code in coming week
  - Have PulsarMon TL2D checking code fully ready ASAP
    - PulsarMon has been a wonderful success!
  - Request a few long beam runs, at different luminosities
    with Pulsar driving alpha auto-reject. Compare TL2D bit by bit
    and study timing performance
  - ACE web page and online monitoring with CO instructions

performance can be further improved of course:
see backup slides on near/long term improvements
It takes time to optimize a new system…and this is a flexible system
Operation readiness in March

- Most important:
  - Run for one week with Alpha driving, Pulsar auto-reject
  - PulsarMon TL2D checking bit by bit, if ok
  - Request run for two weeks with Pulsar driving & alpha auto-reject, with PulsarMon checking TL2D bit by bit, event by event

To make a system more or less working is not hard, to have zero error is hard, to keep it that way could be harder…
Summary

- Pulsar L2 running with system since Feb 02, 2005
- Decision/Control node software working in beam
- Initial study indicates that performance better than Alpha at high luminosity (~ $1 \times 10^{32}$), but a few us behind Alpha at lower luminosity due to long ShowerMax latency (alpha does not wait for SMX data).
  At high luminosity, Muon/XTRP latency is longer than SMX.
- System needs more testing in beam in the next few weeks
- Many ways to improve the performance in near future…
  (all can be done in parasitic mode once in operation)
- Goal is still March, 2005
Backup slides

Just in case people are interested, the rest of slides are for future performance improvements of the Pulsar system
Possible system performance optimization, near term (summer)

- Deliver SMX data on a 3rd S32PCI64
  - send SMX merger data into another S32PCI64
  - CPU no longer waits for SMX data (similar to alpha case)
- Have done a quick test with beam (parasitically) last week, for events do not require SMX, the decision time is ~ few us faster
- Issue to be solved: due to simple PCI handling, introduce extra latency for events that do need SMX (1-2 us)
  - due to: PCI read/write for another S32PCI64…
- Possible solution: modify the firmware to change “request FIFO” to “request RAM”, only configure it once for 4 events
- Contacted CERN experts, to see if there are simpler/quicker ways to improve the interface performance
Change request FIFO → RAM
Same family FPGA used as on Pulsar

S-LINK to PCI-64 interface

http://hsi.web.cern.ch/HSI/s-link/devices/s32pci64
Plan for system performance optimization long term

- Use FILAR cards instead of S32PCI64
  - Remove the final merger, data directly goes into FILAR
  - Replace Reces merger with another FILAR
  - Also allow us to run SLINK faster: 40 MHz → 60 MHz
  - Should reduce the latency by more than ~ 4 us
  - Run in multi-events request mode, expect better performance at higher luminosity/L1A rate

- Already have one FILAR in hand
- Need PCI software work, Kristian already started
- Plan to have Sakari full time on the case soon
FILAR can improve the system latency
→ Higher bandwidth, less latency overhead

64-bit/66MHz PCI bus, four 2 Gbit/s S-LINK channels
Reduced PCI protocol overhead (compare to S32PCI64)

http://hsi.web.cern.ch/HSI/s-link/devices/FILAR
System with FILARs

Pulsar pre-processors

- L1 muon
- L1 XTRP
- L1 trigger
- L2 CAL (CLIST/Iso)
- PreFred
- ShowMax (RECES)

Muon

Cluster

Electron

SVT

Pulsar has two SLINK outputs, one will be used to develop system with FILARs parasitically…
Baseline for operation

To keep things simple:
1. Waiting for Reces data
2. Very simple PCI handling
   - Different from alpha case
   - Not optimal timing performance