Detector modules for the ATLAS SCT endcaps

Lutz Feld*

Institute of Physics, University of Freiburg, Hermann-Herder-Str. 3, D-79104 Freiburg, Germany

For the ATLAS SCT Collaboration

Abstract

1976 double-sided detector modules are needed to equip the endcaps of the silicon microstrip tracker SCT of the ATLAS experiment at the LHC. This paper describes their design and presents results from a series of prototype modules.

© 2003 Elsevier B.V. All rights reserved.

PACS: 29.40.Gx

Keywords: Silicon microstrip detectors; Detector modules; ATLAS; LHC

1. Introduction

A large silicon microstrip detector system (SCT) is currently being constructed for the ATLAS experiment at the CERN Large Hadron Collider LHC [1]. It consists of a central barrel section and two endcaps, allowing for charged particle tracking up to a pseudorapidity of ±2.5. The overall design of this system, and the barrel section in particular are covered in Ref. [2]. Besides the size of the system (61 m² of silicon sensors) the main challenge is the harsh radiation environment at the LHC with an expected equivalent fluence of up to \( 1.3 \times 10^{14} \) 1-MeV neutrons per cm² for the anticipated 10 years of operation.

Each SCT endcap contains 9 disks, which are carbon fiber structures of about 1.2 m diameter. A disk is covered with up to 132 detector modules, arranged in three rings: an ‘outer’ ring of 52 modules and an ‘inner’ ring of 40 modules on one side, and a ‘middle’ ring of 40 modules on the other side (see Fig. 1). In total there will be 1976 detector modules in the SCT endcaps. Modules within a ring as well as different rings overlap in order to minimize gaps in the acceptance. The overlap of neighboring modules is facilitated by mounting and cooling surfaces which are arranged on the centerline of the module. Each module has two mounting surfaces which are both actively cooled for the ‘middle’ and ‘outer’ modules with about 12 cm strip length, while only the main block is cooled for the short ‘inner’ modules with about 6 cm strip length. The cooling system uses the evaporation of \( \text{C}_3\text{F}_8 \) in the cooling pipes on the disks. It can provide cooling down to −30°C, but it is foreseen to operate the SCT at a coolant temperature around −20°C in order to leave some safety margin. Each cooling circuit serves up to 13 modules. The mechanical accuracy of the mounting blocks is driven by the requirement to guarantee sufficient overlap between adjacent

*Tel.: +49-761-203-5753; fax: +49-761-203-5931.
E-mail address: lutz.feld@cern.ch (L. Feld).
modules for inter-module alignment with tracks and to provide good cooling contacts. Each module is serviced by a power tape providing analogue and digital power, as well as slow control signals. Clock and commands are distributed to the module by an optical link. There are two more optical links per module for the transmission of data from the two sides. Therefore, three optical fibers, which are terminated by an opto package containing a PIN diode and two VCSELs, are connected to each module. In order to provide redundancy, each module can receive clock and commands from its neighbor module, and the data from one side of a module can be transmitted through the other side’s optical link.

2. Module design

The ‘middle’ and ‘outer’ modules carry two pairs of wedge shaped silicon microstrip sensors in a back-to-back configuration (see Figs. 2 and 3). The strips in each pair are daisy-chained to form approximately 12 cm long strips. ‘Inner’ modules have just one sensor on each side and about 6 cm strip length. The silicon sensors are single sided with 768 AC-coupled p-type readout strips implanted in n-type silicon of 285 μm thickness. Because of the radial orientation of the strips, their pitch varies with radius between about 55 and 95 μm. The sensors will be able to operate at up to 500 V bias voltage after irradiation, which will be necessary in order to compensate for the radiation induced changes in the silicon. Five different sensor layouts are sufficient to equip the different module types. The delivery of these sensors by Hamamatsu and CiS is almost completed. The sensors on the front and back-side of the module have a stereo angle of 40 mrad such that the coordinate along the module axis can be measured with about 500 μm precision. Perpendicular to the strips the measurement accuracy is of the order of 20 μm, depending on the strip pitch. The in-plane alignment of the sensors in a module is better than 5 μm in the direction perpendicular to the strips, which at least for the initial tracker alignment will allow to treat all modules as identical objects.
The silicon sensors are glued to a support structure consisting of a central bar of Thermal Pyrolytic Graphite (TPG), and aluminum-nitride wings which together with the silicon provide the mechanical stability. The TPG, which has an extremely high thermal conductivity of about 1700 W/m/K in plane runs over the cooling blocks and provides the required cooling of the silicon. After irradiation the silicon sensors show a significant amount of self-heating due to the increased leakage current and operating voltage. Cooling the silicon to a target temperature of −7°C limits the leakage current such that it hardly affects the electronics noise and prevents the risk of thermal runaway. Furthermore, it avoids reverse annealing of the radiation induced change to the effective doping of the silicon. Detailed simulations and measurements on irradiated modules have shown that the modules can be operated safely even at twice the expected radiation damage with a coolant a few degrees below −20°C.

The silicon sensors of a module are read out by 12 custom made front-end ASICs called ‘ABCD3TA’ [3], which are fabricated in the radiation tolerant BiCMOS DMILL process. Each of the 128 channels in a chip contains a preamplifier and shaper with a time constant of about 25 ns, a comparator with a threshold which is adjustable for each individual channel, a digital pipeline which stores the data for about 3 μs until a first level trigger decision is taken, data reduction and readout buffers. In this binary readout scheme the data is reduced to the bare hit information already at the front-end. This simplifies the data transmission and processing. But it is also very demanding on the system performance since any common mode noise has to be kept at negligible levels. The delivery of ASICs is well advanced.

The front-end ASICs are mounted on a double-sided electronics hybrid. It is composed of a 6 layer flexible circuit board with copper traces between polyimide layers, folded around a carbon–carbon substrate (see Fig. 3). The development of this hybrid was difficult and has shown that very low impedance and local decoupling of the analogue and digital supply voltages is critical for a successful operation of ABCD3TA ASICs. Layers 3–6 are reserved for the distribution of power, while signal lines run in layers 1–2. In the wrap around region only two metal layers run from the hybrid front to back side to facilitate the bending of the flex. Typical feature sizes are 75 μm and there are about 3000 microvias establishing connections between different layers. The hybrid supplies a bias voltage of up to 500 V to the silicon sensors. The routing of clock, command and data lines implements the redundancy features mentioned above, and in addition allows to switch-off any of the ASICs without disrupting the operation of the other ASICs. The hybrid carries two more ASICs, called DORIC and VDC, which in conjunction with the opto package are receiver and transmitter for the optical links. The heat generated by the ASICs, up to about 7 W in total, is removed by the highly heat conducting carbon–carbon substrate into the central cooling block. Ceramic thermal plugs under each ASIC establish direct thermal contact between the ASIC and the substrate. The electronics hybrids will be fully assembled and pre-tested in industry.

The hybrid is connected to the detector section of a module only by the 300 μm thick glass fan-ins which—through wire bonds—establish the electrical connection of the detector strips to the ASICs. This configuration implements a thermal split between the hybrid and the silicon sensors which largely avoids heating the sensors by the power dissipation of the ASICs.

![Fig. 4. Equivalent noise charge for each ASIC (chip number on the abscissa) of the 16 prototype modules (marked by different colors). The lower group of modules are of the short ‘inner’ type with about 6 cm strip length, while the other modules are ‘middle’ and ‘outer’ modules with about 12 cm strip length.](image-url)
Sixteen prototype modules of the different types have been assembled at several of the sites which will produce modules for the SCT endcaps. The alignment of these modules was reliably inside specifications. The modules have been subjected to a number of thermo-mechanical tests which—clearly on a still limited statistical basis—show that the thermal properties of the modules are as expected and that they survive the thermal cycles expected during operation without significant permanent deformation. The electrical performance of all modules has been characterized in test boxes. The equivalent noise charge is at or below 1500 electrons for the long, ‘middle’ and ‘outer’ modules, while for the short ‘inner’ modules it is around 900 electrons (see Fig. 4).

A subset of modules has been mounted on a disk sector in order to test the influence of adjacent modules and of the cabling and cooling circuits. No evidence for significant additional noise was found comparing to the individual test-box measurements. A detailed statistical analysis searching for common mode noise showed levels of 100 electrons or below, to be added in quadrature to the single channel random noise, and therefore negligible. These test will be continued with more modules and also with deliberate injection of noise onto cables and pipes in order to improve the robustness of the system.

Due to the binary read-out scheme successful operation of the SCT ultimately requires that thresholds can be set such that good hit efficiency is reached at acceptable levels of noise hit occupancy. We have defined conservative specifications asking for hit efficiency above 99% at a noise occupancy (i.e. probability of a noise hit on a strip in a given event) below $5 \times 10^{-4}$. This has been studied in a test beam with minimum ionizing particles. For non-irradiated modules these specifications are met over a more than 0.5 fC wide window in which the threshold can be varied (Fig. 5, left). After irradiation with $1.6 \times 10^{14}$ 24-GeV-protons per cm$^2$, which corresponds to the expected fluence after about 7 years of operation, there is still an operational window of 0.4 fC, when the detector bias voltage is raised to about 480 V (Fig. 5, middle). After $3.3 \times 10^{14}$ 24-GeV-protons per cm$^2$, corresponding to more than 10 years of operation, the window is very small, which indicates that it will be difficult to meet the specifications after this amount of radiation damage (Fig. 5, right).

The SCT endcap detector modules have passed their final design review, and the collaboration is now preparing for the production of these modules.

References