

Proposal for Checkout and Maintenance of CDF Run IIb L2 Pulsar Boards (and associated support hardware) at PREP

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Uses: replace existing interface boards for Level 2 Trigger Decision Crate. Also used to upgrade several boards in Silicon Vertex Trigger (SVT).

Types of board:

1. 9Ux400mm VIPA Pulsar card with slots for up to 4 mezzanine boards for I/O or memory.
 - a. Total of 95-100 boards will be built. There are 63 in hand as of Sept 2004, balance to be delivered in early 2005.
2. 5 types of custom mezzanine boards
 - a. Hotlink Transmitter (17 already built and tested)
 - b. Hotlink Receiver (17 already built and tested)
 - c. Taxi Transmitter (20 already built and tested)
 - d. Taxi Receiver (45 already built and tested)
 - e. SVT RAM1 (4M x 48bits) (not yet built and tested)
 - f. SVT RAM2 (512K x 24bits) (not yet built and tested)
3. 9Ux120mm transition board which partners with Pulsar board for additional I/O (20 already built and tested)
4. Commercial board purchased for support of CERN SLINK technology
 - a. SLINK Receiver mezzanine card (20 in hand)
 - b. SLINK Transmitter mezzanine card (20 in hand)
 - c. SLINK PCI bus interface card (6 in hand)

Key Features:

1. Pulsar board has 3 large Altera FPGAs (APEX series with BGA mount) with buses between them and to various forms of I/O. I/O can be performed via mezzanine cards, several on board connectors of different types or through P3 (94pin DIN) to transition board.
2. Uses 2 slots in CDF type VIPA crate requiring only +5V power. All other voltages generated on board with DC-DC converters.
3. Board is self testing with capability to operate either as a transmitter or receiver depending on mounted mezzanine cards and loaded firmware.

Design, prototyping, prototype testing, technical support, CDF experimental support:

1. Design of PCB for Pulsar mother board, transition card and mezzanine cards by University of Chicago Electronics shop (Harold Sanders, Mircea Bogdan, and Fukun Tang)
2. Firmware written by contract engineering working for CDF Run IIb upgrade
3. Teststand Software written and supported by Fermilab-CDF department physicists
4. CDF installation, commissioning and 24 hour operational support by Fermilab CDF Department physicists (Ted Liu + postdocs), Univ of Chicago physicists (postdoc + student) and Univ of Pennsylvania physicists (postdoc + student)

Desired PREP Role:

1. Long term maintenance support of boards including testing of failed boards, diagnosing failures, repairing failures, tracking repairs and tracking inventory.
2. Manage and carryout checkout of final run of production Pulsar boards (35) as they arrive from assembly vendor. Production checkout of mezzanine boards to be done by Univ of Chicago.

Teststand:

1. Standalone test of Pulsar will require CDF type VIPA carte, MVME2301, two Pulsars (one under test and one for sourcing/sinking data) and a CDF Testclk module
2. Pulsar functionality tested:
 - a. Test of full internal functionality
 - b. Full I/O functionality of the board with one family of mezzanine board
 - c. Overnight burn-in test
3. Same teststand can be used for test of mezzanine boards.
4. Teststand will have complete software packages provided by CDF.

Background Information:

Additional information can be found at the Pulsar web page:

<http://hep.uchicago.edu/%7Ethliu/projects/Pulsar/>

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