Level 2 Test stand

a set of diagnostic tools (hardware+software)

Outline:

- Why diagnostic tools?
- What are they?
- What can they do for us?
- Progress made so far

Schedule

(Software is not covered in this talk)

Level 2 Review (Dec. 07, 01)

Ted Liu
Why diagnostic tools?

The way we have been debugging the Level 2 decision crate:
very often need to use CDF+Tevatron
→ HUGE amount of work has been done this way by a few hardworking experts!

The idea is to build test stand tools to “replace” CDF and Tevatron,
to make life MUCH easier for EVERYONE.

T. Liu, L2 Review,
Dec. 7th, 01
What are the test tools? -> two types of board:

- **HP scope**
- **Reces**
- **MMB Magic Mystery Board**
- **Sanford XTRP**
- **L2 decision crate**
- **L2 test crate**
- **Logical Analyzer**
- **CDFctrl**
- **Magicbus**
- **TS**
- **L2 inputs**
- **Pulsar**
- **CDFctrl**
- **VME**
- **Hotlink IO**
- **Taxi IO**
- **SVT/XTRP**
- **L1**
- **TS**

T. Liu, L2 Review, Dec. 7th, 01
Goals of Level 2 Test stand

(1) Speed up the debugging process for L2 system:
    Alpha, Mbus, all interface boards
(2) Speed up the optimization process for the soft(firm)ware;
    Alpha code&firmware, interface firmware etc
(3) Fully test the robustness and rate capability of the L2 system
    without the need of beam or high luminosity beam;
(4) Able to capture upstream errors and reproduce them in test stand

(5) Long term maintenance of the system …

Overall goal: make sure we have a robust
L2 system with great performance into Run2b …
Original design for Pulsar board (proposed on Oct 10th):

some changes: use mezzanine cards to reduce the number of boards needed to drive the full system (from 13 to 5); this also means a few more FPGAs per board.

T. Liu, L2 Review, Dec. 7th, 01
Can source data, also can record data from upstream.
PULSAR Design

Can handle up to 16 fiber I/O per board

Front-panel (double width)

Two L1 connectors will stay inside main board

T. Liu, L2 Review, Dec. 7th, 01
4 types Mezzanine card:

- **Hotlink Tx/Rx**: 2
- **Taxi** Tx/Rx: 2

<table>
<thead>
<tr>
<th>Rx type is for:</th>
<th>Hotlink Optical Tx: AMP269051-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>• <strong>Pulsar self-test</strong></td>
<td>Hotlink Optical Rx: AMP269052-1</td>
</tr>
<tr>
<td>• <strong>Record upstream data</strong></td>
<td>(replacement: HFBR-1119T/2119T)</td>
</tr>
</tbody>
</table>

Each card has a few bits ID so that the main board can identify which type is plugged in.

Will add LVDS connectors for CLIST case.

T. Liu, L2 Review,
Dec. 7th, 01
Two L1A case: L1A -> RAM to FIFO -> FIFO -> output
MMB Designer:
Bill Ashmanskas

Proposed in Oct, PCB design was sent out last Friday.

MMB is a Magicbus Analyzer, but it can do much more …

A simple board which can do A LOT

SVT input

SVT output

Master/slave

MagicBus interface

CDFCtrl
Level 2 Test Stand: Board level test

- To just test interface board, one Pulsar + MMB is needed.
- To just test alpha and magicbus, one Pulsar and MMB is needed
- many other options…

Pulsar will provide data inputs and check alpha decisions on the fly, MMB can tell us where is the problem

Data source: Level2_Pulsar
Data sink: Alpha, MMB+Pulsar/GB
Data patterns:
1. hand made
2. derived from MC
3. derived from data bank
4. recorded from upstream, catch errors and reproduce them
Driving the full system: to test the robustness and rate capability, & software/firmware optimization …

On the fly Full Loop Tests with different L1A rate & Event patterns

only 5 Pulsar boards needed to drive the full system
Progress made so far for MMB (Magic Mystery Board)

• Bill proposed the board design on Oct. 10th;

• Bill and UC engineer Mircea finished the PCB design last Friday!

Two MMB PCBs are scheduled to be shipped to UC today…

T. Liu, L2 Review, Dec. 7th, 01
Progress made so far for Pulsar:

• Conceptual Design was proposed on Oct. 10\textsuperscript{th};
• Top level schematics done, design exists for most IO connections;
• initial firmware/simulation started (Natalia Kuznetsova with lots of help from UC chief engineer Harold Sanders);
• Upenn group helped us to purchase all hard to find interface components. And we found a replacement for obsolete hotlink optical Tx/Rx (and tested);
• purchased hotlink evaluation board and have a working hotlink test stand at UC (Natalia), mezzanine card design started;
• Test Stand software work started (Peter Wittich);
• UC engineer (Mircea) started working on Pulsar full time starting this week (after finishing MMB)…
• many help from other experts: Bill Ashmanskas, Karen Byrum, Thurston Chandler, Bob Demaat, Eric James, Matthew Jones, Steve Kuhlmann, Jonathan Lewis, Steve Miller, Monica Tecchio, Peter Wilson …fully supported by UC group, FNAL group and Ops management
Schedule for Level 2 Test Stand

- **Today**: MMB ready
- **Next Feb**: MMB + GhostBuster for initial L2 test stand, can exercise L1, TrackList, Alpha & Mbus already!
- **Pulsar board schematics**
- **Pulsar Firmware/simulation**
- **Mezzanine cards schematics**
- **Test stand software for Pulsar**
- **Layout for Pulsar boards**
- **Layout for mezzanine cards**
  - **1st Mezzanine card**
  - **4th card**
  - **Prototypes ready to test**

T. Liu, L2 Review, Dec. 7th, 01

Next Feb | Next spring