Using Pulsar in SVT?
Part I: Introduction to Pulsar

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For more information on Pulsar board:
http://hep.uchicago.edu/~thliu/projects/Pulsar/

SVT upgrade workshop

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What makes Pulsar potentially useful for SVT upgrade?

- Pulsar is a grandson of SVT (young & energetic!)
- It is made in Chicago (not in China!)

→ Pulsar design was based on SVT design philosophy
→ 1.5 years ago, I spent one month studying SVT architecture & design philosophy before we designed Pulsar…

- As a result, Pulsar is fully compatible with SVT system, with much enhanced capability & flexibility…

- Pulsar is a general purpose 9U VME board for HEP, and fully compatible with ATLAS/CMS DAQ/Trigger
Pulsar is designed to be fully self-testable: at board level as well as system level. For every input/output, there can be an output/input, which allows us to develop & tune an upgrade system standalone.

Pulsar design philosophy:
(1) In God we trust, everything else we test;
(2) One for all, and all for one;
Pulsar design: general purpose board for HEP

9U VME
(VME and CDF ctrl signals are visible to all three FPGAs)

3 Altera APEX 20K400_652 (BGA) FPGAs
502 user IO pins each

Mezz card (CMC) connectors

Data IO

SRAM
128K x 36 bits

Control/Merger

SLINK signal lines

spare lines

Data IO

SRAM

3 APEX20K400-1XV FPGAs on board = 3 Million system gates/80KB RAM per board
2 128K x 36 pipelined SRAMs with No Bus Latency: 1 MB SRAM (~5ns access time)
One possible Pulsar formation

Pulsar pre-processors

Pulsar mergers

PC0

PC1

PC2

PC3

A general purpose DAQ system, or a Level 2 trigger system…
VME interface

- VME interface is based on the same chip on all UC boards:
  - e.g. GB board

- VME interface is available to ALL three FPGAs
- each FPGA has four clock inputs:
  1. CDFCLK;
  2. user defined clock (40 MHz default, for SLINK interface w P3);
  3. Algorithm clock (PLL, tested up to 114MHz);
    OR
  4. Tevatron RF clock (PLL pin on FPGAs)

**Pulsar clocks**
SVT interfaces

1MB SRAM(2 128K x 36): 4 ns access time, pipelined NoBL SRAM

As it is, Pulsar can be used as a powerful GhostBuster board

Pulsar PCB, top side

P2 SVT inter-comm Lines(5): Master & Slave

2 SLINK
Pulsar P3 interface

P3 connection uses P2 style connector, 117 signals mapped to all 5 rows.

Signal Pin map can be made compatible with AM board.

All signals directly visible to Control FPGA.

P3: 117 signal lines

43 signal lines each

Control FPGA

Pulsar PCB, top side
Pulsar P2 inter-communication lines

- Pulsar has five SVT style inter-communication lines on P2 visible to all three FPGAs.

Master and Slave
Level 1 & TS interfaces
all Level 1 trigger bits can be directly available to all FPGAs

TS

L1

64 bits

TS interface with Control FPGA

DataIO FPGA 1

DataIO FPGA 2

SRAM

SRAM

Control FPGA

Pulsar PCB, top side
**SLINK/mezzanine interfaces**

Each mezzanine card has up to 83 user defined signal lines; Four mezzanine card slots up front, 2 in the back of crate. fully compatible with ATLAS DAQ/Trigger

Mezzanine card slots: 5V/3.3V/2.5V power provided by Pulsar
MOAB (Mother of All Boards) for L2 upgrade

Pulsar

Hotlink Tx

Hotlink Rx

Taxi Tx

Taxi Rx

SLINK
LSC/LDC
(ODIN/HOLA)

ANL
SLINK->GBE

AUX Card

Pulsar PCB, top side
PC interface: Gigabit Ethernet / SLINK-PCI or anything one can define on AUX card

- SLINK to Gigabit LSC from ANL, or SLINK LSC/LDC from CERN
- Pulsar is compatible with ATLAS DAQ/trigger: via SLINK
P2 CDF control signals

- Pulsar sees ALL P2 CDF control signals
- Available to ALL three FPGAs
- Can even drive P2 backplane if necessary
Top 10 reasons for Pulsar to be potentially useful for SVT upgrade

• Pulsar is a grandson of SVT (young & energetic);
• Same P2 inter-communication lines (SVT master&slave);
• SVT input is available to all three FPGAs;
• fast large SRAMs (two 128K x 36) already available on board;
• mezzanine card slots can be used for expansion (extra SRAM/FPGA, extra inputs/outputs);
• Back of crate (AUX) card can be used for expansion as well;
• P3 interface can be made compatible with AM board;
• as it is, Pulsar can be used as a powerful GhostBuster board;
• with G-Link mezzanine cards, Pulsar can source/sink SVT system (i.e. SVX fiber data)
• communication within Pulsars and to new L2 decision crate can be done with high bandwidth S-LINK

→ free Pulsars for SVT, this is business within family…😊
→ time to brain storm … see Alex’s talk…
Pulsar Design methodology

A major fraction of the design effort was dedicated to extensive design optimization and verification by using state-of-the-art CAD tools:

- Leonardo Spectrum for VHDL synthesis;
- Altera Quartus II for place and route, FPGA level simulation;
- Mentor Graphics QuickSim for board and multi-board level simulation;
- Interconnect Synthesis tool for trace and cross talk analysis;
- IS_MultiBoard tool for signal integrity checks between motherboard and mezzanine & AUX cards;

we have carefully simulated the board(s) before sending out the prototypes …
Example: Multi-board (9 boards) simulation to verify the design (top level schematics)

It took 1.5 GB memory on a 2GHz/2GB modern PC to simulate 9 boards together at the same time
Pulsar Design methodology

This design methodology allowed us to build flawless prototype boards

The self-test capability of the board design made it possible for us to fully test (all interfaces) the prototype boards within 6 weeks after assembly.

The prototype boards were also tested with on board clock speed up to 114 MHz and no problems were found.

So far, Pulsar has been tested with 
~ 1Billion events (Tx->Rx) without single error…

No single blue wire on all five prototype board (Pulsar + four mezzanine cards)

All firmware (VHDL code) in CVS