L2 Pulsar Test Stand

Overview
Peter Wittich, for the Pulsar Group

http://hep.uchicago.edu/~thliu/projects/Pulsar/
L2 Teststand Requirements

• For long-term maintenance of L2, we need a ‘production test stand’ for all L2 interface boards
  ✔ (What about alpha processor itself ?)

• The testing facility needs to be independent of CDF
  ✔ Need TS, Clock, some source of random L1A’s, but not from official crates

• Facility shouldn’t require board experts for use
Pulsar as L2 Test Stand

• Pulsar is designed to be a test stand for L2 decision crate
• Every L2 sub-system’s data can be *sourced* or *sunk*
• System is *universal* and *modular*
  ✓ L2 system variations are captured in mezzanine cards and firmware
• Self-testing
  ✓ Pulsar can be used to test itself by sinking and sourcing its own data
# Hardware Requirements

- Pulsar must be able to talk to all L2 subsystems
  - ✓ Level 1
  - ✓ Clustering
  - ✓ Tracks
  - ✓ ShowerMax
  - ✓ Muon
- No direct communication with the $\alpha$ board(s)
- No direct Magic Bus interface (MMB already fills this role)

## Glossary for non-experts

<table>
<thead>
<tr>
<th>L1</th>
<th>L1Int$^1$</th>
<th>Aux</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clustering</td>
<td>CList$^2$, IsoList$^3$</td>
<td></td>
</tr>
<tr>
<td>Tracking</td>
<td>SVTList$^4$, XTRP$^5$</td>
<td></td>
</tr>
<tr>
<td>Shower Max</td>
<td>RECES$^6,7,8,9$ (x4)</td>
<td>Aux</td>
</tr>
<tr>
<td>Muon</td>
<td>MuonList$^{10}$ (name?)</td>
<td></td>
</tr>
</tbody>
</table>

$^1$ Seven types of boards (incl. $\alpha$)
Testing Requirements

• Self-contained testing of L2 Decision crate
  ✓ No more “CDF pulser” - test L2 w/o rest of CDF
  ✓ Realistic data sizes and latency

• Be a self-testable system
  ✓ This requirement meshes nicely with the next testing feature

• Record data from upstream
  ✓ Understand problems with upstream systems
  ✓ Catch data for later playback

→ More details in firmware talk later…
L2 Decision Crate - Cables

Magic bus (128 bits)

Track data

cluster data

ROC Tracer

Alphas X 4

L2 crate inputs

One SVT Cable each

6 fiber (hotlink)

1 LVDS cable

12 fibers (Taxi)

16 fibers (hotlink)

7 fibers (taxi)
## Level 2 Data Paths

<table>
<thead>
<tr>
<th></th>
<th>SVT</th>
<th>XTRP</th>
<th>L1</th>
<th>CLIST</th>
<th>ISO</th>
<th>Muon</th>
<th>Reces</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Incoming data</strong></td>
<td>30Mhz</td>
<td>7.6Mhz</td>
<td>7.6Mhz</td>
<td>20Mhz</td>
<td>12Mhz</td>
<td>30Mhz</td>
<td>7.6 Mhz</td>
</tr>
<tr>
<td><strong>Clock rate</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>cdfclk</td>
</tr>
<tr>
<td><strong>Interface hardware</strong></td>
<td>SVT cable</td>
<td>SVT cable</td>
<td>L1 cable</td>
<td>Hotlink+fiber</td>
<td>Taxi+fiber</td>
<td>Hotlink+fiber</td>
<td>Taxi+fiber</td>
</tr>
<tr>
<td><strong>data size range</strong></td>
<td>150bits/trk</td>
<td>21 bits/trk</td>
<td>96 bits/evt</td>
<td>46bits/clu</td>
<td>145bits/clu</td>
<td>11Kbits/evt</td>
<td>1.5Kb/evt</td>
</tr>
<tr>
<td><strong>Latency range</strong></td>
<td>~10-100us</td>
<td>~1us - 10us</td>
<td>~132 ns</td>
<td>~1-20us</td>
<td>~few us</td>
<td>~1-5 us</td>
<td>~ 6 us</td>
</tr>
<tr>
<td><strong>Fixed or variable</strong></td>
<td>variable</td>
<td>variable</td>
<td>fixed</td>
<td>variable</td>
<td>variable</td>
<td>fixed</td>
<td>fixed</td>
</tr>
<tr>
<td><strong>data length?</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Data with Buffer#?</strong></td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td><strong>EOE with data?</strong></td>
<td>yes</td>
<td>yes</td>
<td>-</td>
<td>no</td>
<td>no</td>
<td>yes</td>
<td>-</td>
</tr>
<tr>
<td>(or from separate path?)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>B0 marker?</strong></td>
<td>BC#</td>
<td>BC#</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td><strong>Data gap within</strong></td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>no</td>
<td>yes</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>one event?</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Flow control ?</strong></td>
<td>Not used</td>
<td>not used</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>no</td>
</tr>
</tbody>
</table>

* *Latency range also depends on L1A history …*
**Tester Functional Requirement**

**Single Board tester:**
- Wait for L1A
- On L1A, wait a characteristic delay time
- Send data to “client”

**System Tester:**
- Wait for L1A
- On L1A, wait a characteristic delay time *for each system*
- Send data to “clients”

In either case, data is then sent through $\alpha$, for manipulation or verification.
Test Stand Example

Simple Single-board Testing Overview

- Pulsar sources data, $\alpha$ sinks it
- Check data integrity on alpha
- Tests full data path
- Needs a dedicated test-stand alpha
Test stand w/o dedicated alpha

- The Magic Mystery Board (MMB) gives the test stand MagicBus connectivity
- This setup can be used if we can’t spare α’s

Magic bus or TDC backplane

<table>
<thead>
<tr>
<th>ROC</th>
<th>TRACER</th>
<th>or TESTCLK?</th>
</tr>
</thead>
</table>

Magicbus Analyzer

data input
Pulsar Baseline

Level2_Pulsar baseline design

- Four mezzanine cards to abstract the connections for optical transceivers
- Track, L1 connections explicit on board
- VME control
- Sees CDF control lines

Pulsar: Pulser and Recorder (as Level 2 test stand tools)
Use spare Pulsar resources to make a more general board.

• Add signal traces to P3 connector for SLINK IO
  ✓ This allows Pulsar to interface directly with a PC via commercially available SLINK to PCI cards
  ✓ These capabilities will be very useful as a general purpose diagnostic tool

• Make L1 and SVT/XTRP inputs visible to all 3 FPGA’s instead of just one.

Note: The mezzanine card connector is already compatible with SLINK mezzanine cards, as both of them follow CMC standards. This allows us to test Pulsar prototype with SLINK test tools as well.

Since these modifications are simple, it doesn’t hurt to add them.
Pulsar Enhanced

- Distribute L1, tracks
- Add Slink to P3
- Assure mez cards’ compatibility with S-Link

From test stand tool to a more general purpose board: only need a few minor changes
The mezzanine card connectors can be used either for user I/O or SLINK cards.
Types of Pulsars

• Pulsar Tx
  ✓ Intended for data transmission
    • Has Tx mezzanine cards, firmware
  ✓ Pulsar board w/o P3: can plug into Magic Bus crate (but cannot communicate with MB)

• Pulsar Rx
  ✓ Intended for data reception
    • Has Rx mezzanine cards, firmware
  ✓ Fully stuffed (“P2-style”) P3 connector- can communicate via S-Link to PC, other Pulsar

• Boards are physically different to allow plug-in to Magic Bus crates (convenience)
Test Stand Setup

- Part of larger CDF electronics test stand
- The test stand will require four crates
  - Magic bus crate (Pulsar Tx)
  - CDF cal crate (Pulsar Rx)
  - Clock Crate
  - Ts Crate
- Complete stand-alone operation
- Allows board-level and system-level tests.
Trigger Room Set-up

- Use empty L2 controller crate in the trigger room
- Save data
  - To diagnose other subsystem problems
  - For recording and later play-back

→ Total system requirements at FNAL: 9 Pulsar boards
Coming next ....

- Pulsar mezzanine card design
  ✔ Natalia
- Pulsar mother board design
  ✔ Mircea
- Pulsar firmware
  ✔ Me again...
- Discussion