ELECTRONICS

Physics 226 - Spring Quarter, 2009 - University of Chicago

REVIEW EXERCISES DUE THURSDAY, JUNE 4

1. (Horowitz and Hill, 8.14, page 493): Find logic to perform multiplication of two 2-bit unsigned numbers (i.e., each 0 to 3), producing a 4-bit result. Hint: Use a separate Karnaugh map for each output bit.

Implement the corresponding circuit with any combination of gates. One solution involves several AND gates, one XOR gate, and one inverter.

2. (Horowitz and Hill, 8.25, page 514): Design a synchronous 2-bit UP/DOWN counter: It has a clock input, and a control input (U/D'); the outputs are the two flip-flop outputs Q_1 and Q_2. If U/D' is high, it goes through a normal binary counting sequence; if LOW, it counts backward – $Q_2Q_1 = 00,\ 11,\ 10,\ 01,\ 00, \ldots$.

One solution involves two D-type flip-flops, two XOR gates, and an inverter.

3. Denote a prime from 1 to 15 by the four-bit sequence $A_4A_3A_2A_1$, where A_4 is the most significant bit (8-bit) and A_1 is the least significant bit (1-bit). Make a Karnaugh map with A_4A_3 along the horizontal axis and A_2A_1 along the vertical axis and denote a prime by 1, non-prime by 0. Find a combinatorial logic which determines using the four bits whether the number is prime. You need not draw the gates which implement this logic.