

# CDF Level 2 trigger upgrade, CLUSTER PULSAR board testing

Wojciech Fedorko

10<sup>th</sup> March 2004

Physics 335

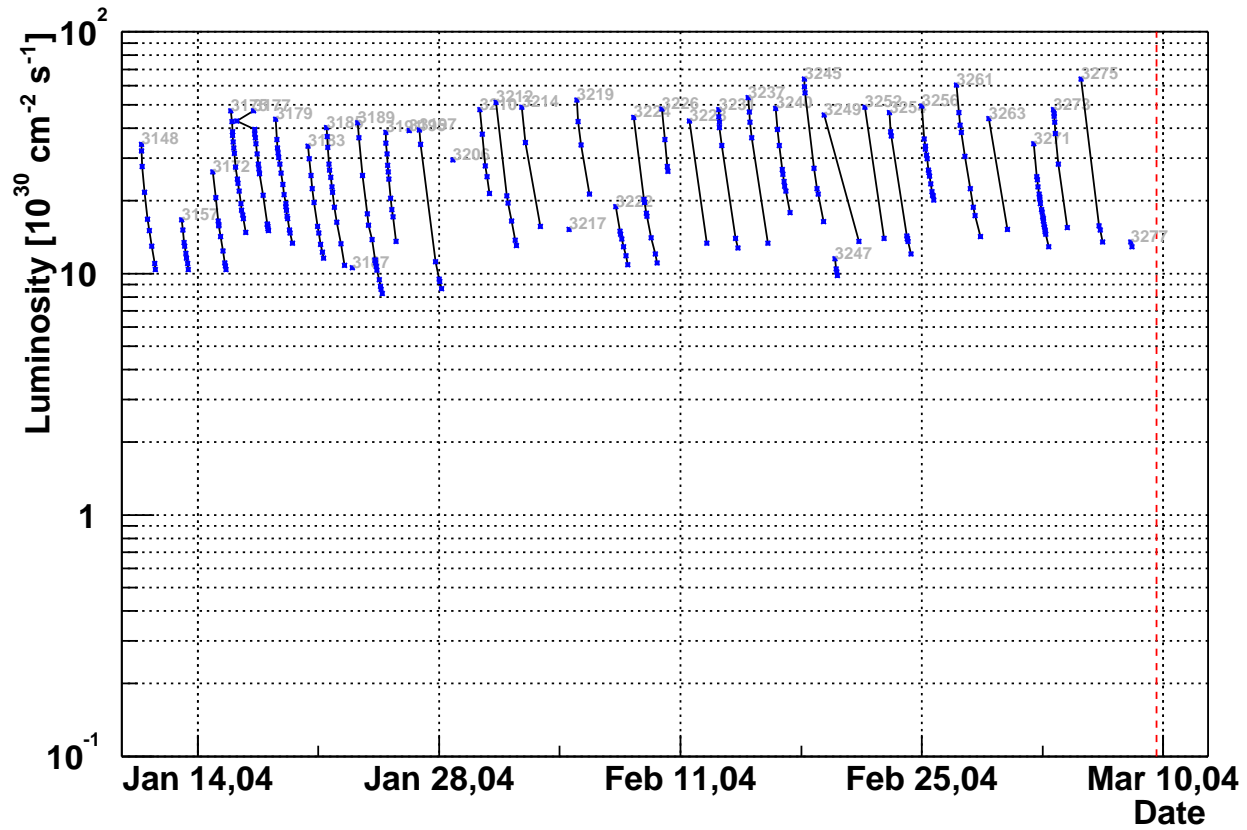
Project Supervisor: Young-Kee Kim

- Overview of the trigger at CDF
- **Trigger upgrade plan**
- **Parasitic running in the real system.**
  - **Old and new fanout boards**

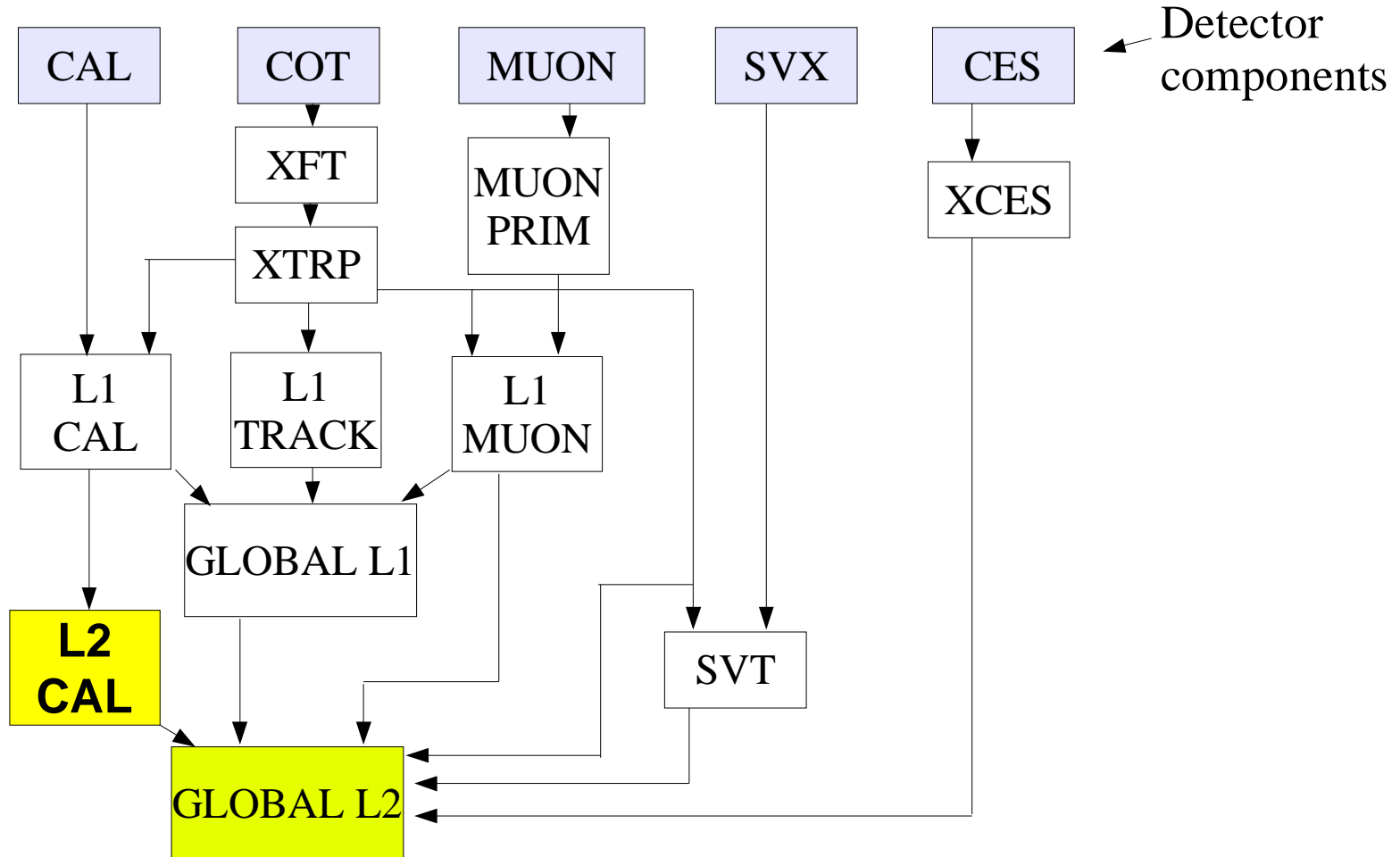
- Trigger system is designed to cut down the data flow to manageable levels
- Decision if the event is to be kept or thrown away is made based on presence of interesting objects in the event: jets, high  $p_T$  electrons, b-tags etc.
- Decision is made in three stages- more sophisticated (and slower) processing is performed at each level
- Luminosity climbing: Level 2 will not be able to cope with this increase

# Luminosity (Last 60 days)

Wed Mar 10 08:15:54 2004



Our responsibility is the L2 calorimetry trigger





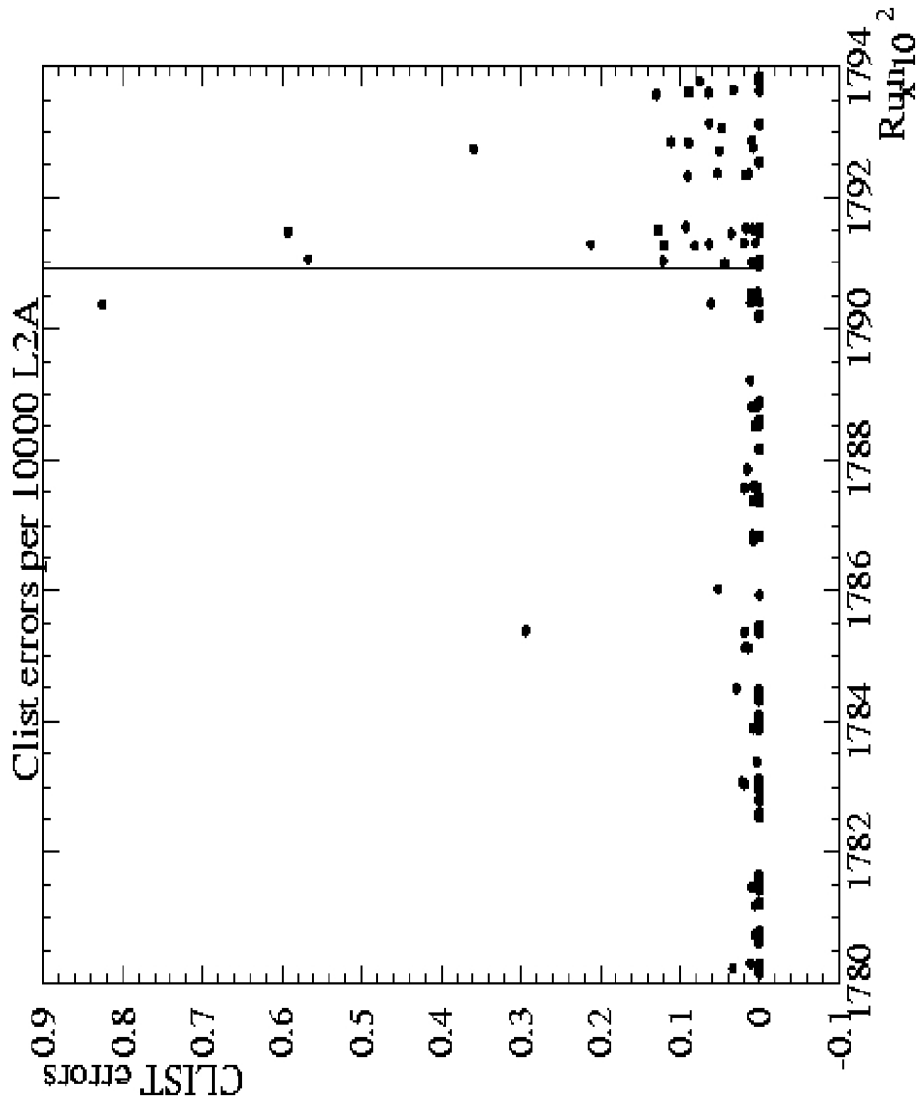
- The best test for a new piece of hardware is 'parasitic running'
  - Split the incoming signals and run the board in parallel to the normal system
- We already had fiber splitters for the CLIST board
- LVDS splitter was needed

We had an (ancient) 'L1' fanout board which also used an LVDS standard

I adapted the board to the LVDS splitting.

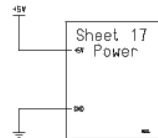
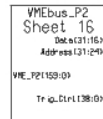
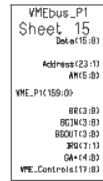
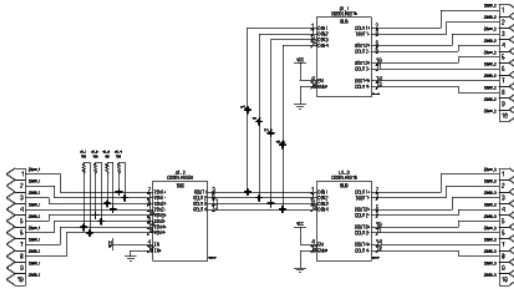
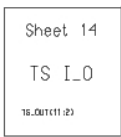
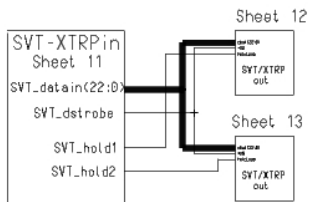
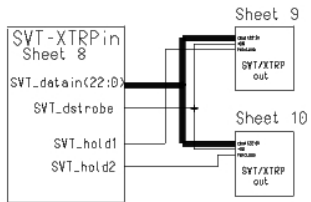
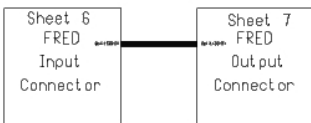
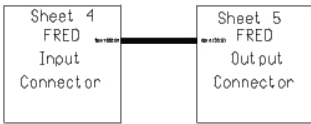
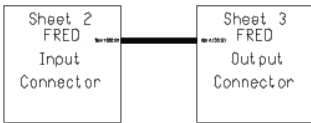
Board was thoroughly tested at the teststand at Fermilab

We plugged the board in the CDF trigger room and were able to use it for testing the CLIST PULSAR



Decision was made to make a new fanout board:

- Handle all LVDS signals we will ever need for parasitic running:
  - 3x L1
  - 2x SVT/XTRP
  - 1x TS
  - 1x 10pin LVDS (<- Needed for CLIST)
- Handles back signals (SVT\_hold; TS L2\_A L2\_R) properly - with use of jumpers one can configure the board as just pass through.



UNIVERSITY OF CHICAGO  
Electronics Design Group

Design MB/TL  
Check  
01/22/84  
TITLE Level2 Fanout  
Top Level  
Drawing Number 2541  
Sheet 1 of 17

MGC File Geometries Setup Setup Placement Setup Routing Setup Hispeed Check Report Properties View Help Support

BO\$9UVME V A I O R

Selected: 0 Check On Hispeed Check On Components: 570 (0) None 0.008  
Delta: 7.2, -1.2 Abs: 9.5, -15.25 In. Grid: X 0.05, Y 0.05 SIGNAL 1

SESSION ? HELP ?  
PLACE ROUTE  
AUTO PLACE AUTO ROUTE  
DYNAMIC EDITOR... AREAFILL  
CHANGE DEF TEXT  
HISPEED

PCB Level 1 - FanOut board  
DATE: 11/11/2009 10:00:00 AM  
DESIGNER: J. J. J. J. J.  
PROJECT: BO\$9UVME  
FILE: BO\$9UVME.PCB  
DATE: 11/11/2009 10:00:00 AM  
DESIGNER: J. J. J. J. J.  
PROJECT: BO\$9UVME  
FILE: BO\$9UVME.PCB

PCB Level 2 - FanOut board  
DATE: 11/11/2009 10:00:00 AM  
DESIGNER: J. J. J. J. J.  
PROJECT: BO\$9UVME  
FILE: BO\$9UVME.PCB

COOPER M3-2500

```

i $unselect_all(@fills_absent, @geom_attributes_absent, @components_absent, @gates_absent,
rdrops_absent, @arcs_absent, @circles_absent, @lines_absent, @polygons_absent);
// Note: Objects unselected = 0. (from: Idea/Librarian/Select 0D)

```

- Design and layout were done at the electronic shop
- My job was QA for the board
  - I have run board simulations in 'QuickSim'
  - Checked connection list
- Designs will be sent out to manufacturer shortly

Trace



0.0 800.0 1600.0 2400.0 3200.0 4000.0 4800.0 5600.0 6400.0 7200.0  
Time (ns)

## PLANS FOR NEXT QUARTER:

- Hope to test the new board (should have it mid Apr) (?)
- Writing tools for data analysis
  - Some tools already written by Vadim Rusu (postdoc)
  - I want to expand on these- we need sophisticated monitoring.
    - Displaying clusters reconstructed by the board in comparison to board simulation; comparing counts positions, energies etc...