A 15 GSa/s, 1.5 GHz Bandwidth Waveform Digitizing ASIC

Eric Oberla\textsuperscript{a}, Hervé Grabas\textsuperscript{a,1}, Jean-Francois Genat\textsuperscript{b,2}, Henry Frisch\textsuperscript{a}, Kurtis Nishimura\textsuperscript{b,3}, Gary Varner\textsuperscript{b}

\textsuperscript{a}Enrico Fermi Institute, University of Chicago; 5640 S. Ellis Ave., Chicago IL, 60637
\textsuperscript{b}University of Hawai’i at Manoa; Watanabe Hall, 2505 Correa Rd., Honolulu HA

Abstract

The PSEC4 custom integrated circuit was designed for the recording of fast waveforms for use in large-area time-of-flight detector systems. The ASIC has been fabricated using the IBM-8RF 0.13 \( \mu \)m CMOS process. On each of 6 analog channels, PSEC4 employs a switched capacitor array (SCA) 256 samples deep, a ramp-compare ADC with 10.5 bits of effective resolution, and a serial data readout with the capability of region-of-interest windowing to reduce dead time. The sampling rate can be adjusted between 4 and 15 Gigasamples/second [GSa/s] on all channels and is servo-controlled on-chip with a low-jitter delay-locked loop (DLL). The input signals are passively coupled on-chip with a -3dB analog bandwidth of 1.5 GHz. The power consumption in quiescent sampling mode is less than 50 mW/chip; at a sustained trigger and readout rate of 50 kHz the chip draws 100 mW. After fixed-pattern pedestal subtraction, the uncorrected differential non-linearity is 0.15% over an 800 mV dynamic range. With a linearity correction, a full 1 V dynamic range is available. The sampling timebase has a fixed-pattern non-linearity with an RMS of 13%, which can be calibrated for precision waveform feature extraction and picosecond-level timing resolution. The first experimental application to the front-end readout of large-area Micro-Channel Plate (MCP) photodetectors is presented.

Keywords:
Waveform sampling, ASIC, Integrated Circuit, Analog-to-Digital, Switched Capacitor Array

1. Introduction

We describe the design and performance of PSEC4, a \( \geq 10 \) Gigasample/second [GSa/s] waveform sampling and digitizing Application Specific Integrated Circuit (ASIC) fabricated in the IBM-8RF 0.13 \( \mu \)m complementary metal-oxide-semiconductor (CMOS) technology. This compact ‘oscilloscope-on-a-chip’ is designed for the recording of radio-frequency (RF) transient waveforms with signal bandwidths between 100 MHz and 1.5 GHz.

1.1. Background

The detection of discrete photons and high-energy particles is the basis of a wide range of commercial and scientific applications. In many of these applications, the relative arrival time of an incident photon or particle is best measured by extracting features from the full waveform at the detector output [1, 2]. Additional benefits of front-end waveform sampling include the detection of pile-up events and the ability to filter noise or poorly formed pulses.

For recording ‘snapshots’ of transient waveforms,
switched capacitor array (SCA) analog memories can be used to sample a limited time-window at a relatively high rate, but with a latency-cost of a slower readout speed [3, 4]. These devices are well suited for triggered-event applications, as in many high energy physics experiments, in which some dead-time can be afforded on each channel. With modern CMOS integrated circuit design, these SCA sampling chips may be compact, low power, and relatively low cost per channel [4].

Over the last decade, sampling rates in SCA waveform sampling ASICs have been pushed to several GSa/s with analog bandwidths of several hundred MHz [5]. As a scalable front-end readout option coupled with the advantages of waveform sampling, these ASICs have been used in a wide range of experiments; such as high-energy physics colliders [6], gamma-ray astronomy [7, 8], high-energy neutrino detection [9, 10], and rare decay searches [11, 12].

1.2. Motivation

A natural extension to the existing waveform sampling ASICs is to push design parameters that are inherently fabrication technology limited. Parameters such as sampling rate and analog bandwidth are of particular interest considering the fast risetimes ($\tau_r \sim 60$-500 ps) and pulse widths (FWHM $\sim 200$ ps - 1 ns) of commercially available micro-channel plate (MCP) and silicon photomultipliers [13, 14]. These and other fast photo-optical or RF devices require electronics matched to speed of the signals.

The timing resolution of discrete waveform sampling is intuitively dependent on three primary factors as described by Ritt$^4$ [15]:

$$\sigma_t \propto \frac{\tau_r}{(SNR)\sqrt{N_{\text{samples}}}} \quad (1)$$

where $SNR$ is the signal-to-noise ratio of the pulse, $\tau_r$ is the 10-90% rise-time of the pulse, and $N_{\text{samples}}$ is the number of independent samples on the rising edge within time $\tau_r$. The motivation for oversampling above the Nyquist limit is that errors due to uncorrelated noise, caused both by random time jitter and charge fluctuations, are reduced by increasing the rising-edge sample size. Accordingly, in order to preserve the timing properties of analog signals from a fast detector, the waveform recording electronics should 1) be low-noise, 2) match the signal bandwidth, and 3) have a reasonably fast sampling rate.

1.3. Towards 0.13 $\mu$m CMOS

The well-known advantages of reduced transistor feature size include higher clock speeds, greater circuit density, lower parasitic capacitances, and lower power dissipation per circuit [16]. The sampling rate and analog bandwidth of waveform sampling ASICs, which depend on clock speeds, parasitic capacitances, and interconnect lengths, are directly enhanced by moving to a smaller CMOS technology. Designing in a smaller technology also allows clocking of an on-chip analog-to-digital converter (ADC) at a faster rate, reducing the chip dead-time.

With the advantages of reduced transistor feature sizes also comes increasingly challenging analog design issues. One issue is the increase of leakage current. Leakage is enhanced by decreased source-drain channel lengths, causing subthreshold leakage ($V_{GS} < V_{TH}$), and decreased gate-oxide thickness, which promotes gate-oxide tunneling [17]. Effects of leakage include increased quiescent power dissipation and potential non-linear effects when storing analog voltages.

Another design issue of deeper sub-micron technologies is the reduced dynamic range [17]. The available voltage range is given by ($V_{DD}$-$V_{TH}$), where $V_{DD}$ is the supply voltage and $V_{TH}$ is the threshold, or ‘turn-on’, voltage for a given transistor. For technologies above 0.1 $\mu$m, the ($V_{DD}$-$V_{TH}$) range is decreased with downscaled feature sizes to reduce high-field effects in the gate-oxide [17]. In the 0.13 $\mu$m CMOS process, the supply voltage $V_{DD}$ is 1.2 V and the values of $V_{TH}$

---

$^4$Assuming Shannon-Nyquist is fulfilled
range from 0.42 V for a minimum-size transistor (gate length 120 nm) to roughly 0.2 V for a large transistor (5 µm) [18, 19].

The potential of waveform sampling design in 0.13 µm CMOS was shown with two previous ASICs. A waveform sampling prototype achieved a sampling rate of 15 GSa/s and showed the possibility of analog bandwidths above 1 GHz [20]. Leakage and dynamic range studies were also performed with this chip. In a separate 0.13 µm ASIC, fabricated as a test-structure chip, a 25 GSa/s sampling rate was achieved using low V$_{TH}$ transistors [21]. The performance and limitations of these chips led to the optimized design of the PSEC4 waveform digitizing ASIC. The fabricated PSEC4 die is shown in Figure 1.

In this paper, we describe the PSEC4 architecture (§2), experimental performance (§3), and a first application to the front-end readout of large-area, picosecond resolution photodetectors (§4).

2. Architecture

An overview of the PSEC4 architecture and functionality is shown in Figure 2. For clarity, this block diagram shows one of six identical signal channels. A PSEC4 channel is a linear array of 256 sample points and a threshold-level trigger discriminator. Each sample point in the array is made from a switched capacitor sampling cell and an integrated ADC circuit as shown in Figure 3.

To operate the chip, a field-programmable gate array (FPGA) is used to provide timing control, clock generation, readout addressing, data management, and general configurations to the ASIC. Several analog voltage controls are also required for operation, and are provided by commercial digital-to-analog converter (DAC) chips.

Further details of the chip architecture, including timing generation (§2.1) sampling and triggering (§2.2), analog-to-digital conversion (§2.3), and data readout (§2.4), are outlined in the following sections.

2.1. Timing Generation

The sampling signals are generated with a 256-stage Voltage-Controlled Delay Line (VCDL), in which the individual stage time delay is adjustable by two complementary voltage controls. Each stage in the VCDL is an RC delay element made from a CMOS current-starved inverter. The inverse of the time delay between stages sets the sampling rate. Rates of up to 17 GSa/s are possible with PSEC4 as shown in Figure 4. The stability of the sampling rate is negatively correlated with the slope magnitude as the VCDL becomes increasingly sensitive to noise. The slowest stable sampling rate is ~4 GSa/s.

A 'write strobe' signal is sent from each stage of the VCDL to the corresponding sampling cell in each channel. The write strobe passes the VCDL-generated sampling rate to the sample-and-hold switch of the cell as shown in Figure 3. To allow the sample cell enough time to fully charge or discharge when sampling, the write strobe is extended to a fixed duration of 8× the individual VCDL delay stage. In sampling mode, a block of 8 adjacent SCA sampling cells are continuously tracking the...
Figure 2: A block diagram of PSEC4 functionality. The RF-input signal is AC coupled and terminated in 50Ω off-chip. The digital signals (listed on right) are interfaced with an FPGA for PSEC4 control. A 40 MHz write clock is fed to the chip and up-converted to ∼10 GSa/s with a 256-stage voltage-controlled delay line (VCDL). A ‘write strobe’ signal is sent from each stage of the VCDL to the corresponding sampling cell in each channel. The write strobe passes the VCDL-generated sampling rate to the sample-and-hold switches of each SCA cell. Each cell is made from a switched capacitor sampling cell and integrated ADC register, as shown in Figure 3. The trigger signal ultimately comes from the FPGA, in which sampling on every channel is halted and all analog samples are digitized. The on-chip ramp-compare ADC is run with a global analog ramp generator and 1 GHz clock that are distributed to each cell. Once digitized, the addressed data are serially sent off-chip on a 12-bit bus clocked at up to 80 MHz.

Figure 3: Simplified schematic of the ‘vertically integrated’ PSEC4 cell structure. The sampling cell input, V_{in}, is tied to the on-chip 50Ω input microstrip line. Transistors T1 and T2 form a dual-CMOS write switch that facilitates the sample-and-hold of V_{in} on C_{sample}, a 20 fF capacitor. The switch is toggled by the VCDL write strobe while sampling (Figure 2) or a ASIC-global trigger signal when an event is to be digitized. When the ADC is initiated, a global 0.0-1.2 V analog voltage ramp is sent to all comparators, which digitizes the voltage on C_{sample} using a fast ADC clock and 12-bit register. To send the digital data off-chip, the register is addressed using Read_enable.
input signal.

To servo-control the VCDL at a specified sampling rate and to compensate for temperature effects and power supply variations, the VCDL can be delay-locked on chip. The VCDL forms a delay-locked loop (DLL) when this servo-controlled feedback is enabled. The servo-control circuit is made of a dual phase comparator and charge pump circuit to lock both the rising and falling edges of the write clock at a fixed one-cycle latency [22]. A loop-filter capacitor is installed externally to tune the DLL stability.

With this DLL architecture, a write clock with frequency $f_{in}$ is provided to the chip, and the sampling is started automatically after a locking time of several seconds. The nominal sampling rate in GSa/s is set by $0.256 \cdot f_{in}$ [MHz], and the sampling buffer depth in nanoseconds is given by $10^3/f_{in}$ [MHz$^{-1}$]. A limitation of the PSEC4 design is the relatively small recording depth at high sampling rates due to the buffer size of 256 samples.

2.2. Sampling and Triggering

A single-ended, 256-cell SCA was designed and implemented on each channel of PSEC4. Each sampling cell circuit is made from a dual CMOS write switch and a 20 fF sampling capacitor as shown in Figure 3. During sampling, the write switch is toggled by the write strobe from the VCDL. To record an event, an external trigger, typically from an FPGA, overrides the sampling and opens all write switches, holding the analog voltages on the capacitor for the ADC duration ($\leq 4 \mu s$).

The PSEC4 has the capability to output a threshold-level trigger bit on each channel. The internal trigger is made from a fast comparator, which is referenced to an external threshold level, and digital logic to latch and reset the trigger circuit. To form a PSEC4 trigger, the self-trigger bits are sent to the FPGA, which returns a global trigger signal back to the chip. Triggering interrupts the sampling on every channel, and is held until the selected data are digitized and read out.

2.3. ADC

Digital conversion of the sampled waveforms is done on-chip with a single ramp-compare ADC that is parallelized over the entire ASIC$^5$. Each sample cell has a dedicated comparator and 12 bit register as shown in Figure 3. In this architecture, the comparison between each sampled voltage ($V_{sample}$) and a global ramping voltage ($V_{ramp}$), controls the clock enable of a 12-bit register. When $V_{ramp} > V_{sample}$, the register clocking is disabled, and the 12-bit word, which has been encoded by the ADC clock frequency and the ramp duration below $V_{sample}$, is latched and ready for readout.

Embedded in each channel is a 5-stage ring oscillator that generates a fast digital ADC clock, adjustable between 200 MHz and 1.4 GHz. The ADC conversion time, power consumption, and resolution may be configured by adjusting the ramp slope or by tuning the ring oscillator frequency.

2.4. Readout

The serial data readout of the register bits is performed using a shift register ‘token’ architecture, in which a read_enable pulse is passed sequentially along the ADC register array. To reduce the chip readout latency, a limited selection of PSEC4’s 1536 registers can be read out. Readout addressing is done by selecting the channel number and a block of 64 cells. While not completely random access, this scheme permits a considerable reduction in dead time. At a maximum rate of 80 MHz, the readout time is $0.8 \mu s$ per 64-cell block.

The readout latency is typically the largest contributor to the dead-time of the chip. The ADC conversion time also adds up to $4 \mu s$ of latency per triggered event. These two factors limit the sustained trigger rate to $\sim 200$ kHz/channel or $\sim 50$ kHz/chip.

$^5$An overview of this ADC architecture can be found in reference [23].
Figure 4: Sampling rate as a function of VCDL voltage control. Good agreement is shown between post layout simulation and actual values. Rates up to 17 GSa/s are achieved with the free-running PSEC4 VCDL. When operating the VCDL without feedback, the control voltage is explicitly set and the sampling rate is given by $17.7 \left(1 - 0.018 \exp[5.91 \times \text{Voltage Control}]\right) \text{[GSa/s]}$. Typically, the servo-locking will be enabled and the VCDL is run as a delay-locked loop (DLL). In this case, the sampling rate is automatically set by the input write clock frequency.

Figure 5: The PSEC4 evaluation board. The board uses a Cyclone III Altera FPGA (EP3C25Q240) and a USB 2.0 PC interface. Custom firmware and acquisition software was developed for overall board control. The board uses +5 V power and draws <500 mA, either from a DC supply or the USB interface.

3. Performance

Measurements of the PSEC4 performance have been made with several chips on custom evaluation boards shown in Figure 5. The sampling rate was fixed at a nominal rate of 10.24 GSa/s. Here we report on bench measurements of linearity (§3.1), analog leakage (§3.2), noise (§3.3), power (§3.4), frequency response (§3.5), sampling calibrations (§3.6), and waveform timing (§3.7). A summary table of the PSEC4 performance is shown in §3.8.

3.1. Linearity and Dynamic Range

The input dynamic range is limited by the 1.2 V core voltage of the 0.13 µm CMOS process [18]. To enable the recording of signals with pedestal levels that exceed this range, the input is AC coupled and a DC offset is added to the 50 Ω termination. This is shown in the Figure 2 block diagram, in which
the DC offset is designated by $V_{\text{ped}}$. The offset level is tuned to match the input signal dynamic range to that of PSEC4.

The PSEC4 response to a linear pedestal scan is shown in Figure 6. A dynamic range of 1 V is shown, as input signals between 100 mV and 1.1 V are fully coded with 12 bits. A differential non-linearity (DNL) of better than 0.15% is shown for most of that range. The linearity and dynamic range near the voltage rails are limited due to transistor threshold issues in the comparator circuit.

The DNL of this response, shown by the linear fit residuals in Figure 6, can be corrected by creating an ADC count-to-voltage look-up-table (LUT) that maps the input voltage to the PSEC4 output code. The raw PSEC4 data is converted to voltage and ‘linearized’ using this LUT.

### 3.2. Sample Leakage

When triggered, the write switch (Fig. 3) is ideally an open circuit, but sub-threshold conduction of transistors T1 and T2 provide a path for charge leakage from the 20 fF sampling capacitor. This forms a ‘leakage current’, in which the charge travels back to the input line and returns to ground through the 50 Ω termination. To reduce leakage effects, the analog-level storage time on the sampling capacitors is minimized.

To measure the leakage current, a 400 mV, 100 ns wide pulse was sent to a PSEC4 channel. Since the sampling window is 25 ns, each SCA cell sampled the 400 mV transient level. After triggering, the delay of the ADC start signal was incremented at 10 μs intervals, which correspondingly increased the analog storage time on the sampling capacitors. The difference between the nominal 400 mV input and the PSEC4 digitized level was recorded and is shown in Figure 7. As expected for an RC-discharge, a decaying exponential ($\tau = 167 \, \mu s$) fits the data with good agreement.

In normal operation, the ADC is started immediately after a trigger is registered so that the analog voltage hold time is limited to the ADC conversion time. To log the full 12 bits at an ADC clock rate of 1 GHz, the maximum conversion time is 4 μs during which a small amount of charge leakage may occur. This is shown in the red-hatched
After fixed-pattern pedestal correction and event-by-event baseline subtraction, which removes low-frequency noise contributions, the PSEC4 electronic noise is measured to be $\sim 700 \mu V$ RMS on all channels as shown in Figure 8. The noise figure is dominated by broadband thermal noise on the 20 fF sampling capacitor, which contributes $450 \mu V$ (RMS 60 electrons) at 300 K. Other noise sources include the ADC ramp generator and comparator. The noise corresponds to roughly 3 least significant bits (LSBs), reducing the effective resolution of the device to 10.5 bits over the dynamic range.

### 3.3. Noise

After fixed-pattern pedestal correction and event-by-event baseline subtraction, which removes low-frequency noise contributions, the PSEC4 electronic noise is measured to be $\sim 700 \mu V$ RMS on all channels as shown in Figure 8. The noise figure is dominated by broadband thermal noise on the 20 fF sampling capacitor, which contributes $450 \mu V$ (RMS 60 electrons) at 300 K. Other noise sources include the ADC ramp generator and comparator. The noise corresponds to roughly 3 least significant bits (LSBs), reducing the effective resolution of the device to 10.5 bits over the dynamic range.

### 3.4. Power

The power consumption is dominated by the ADC, which simultaneously clocks 1536 ripple counters and several hundred large digital buffers at up to 1.4 GHz. The total power draw per chip as a function of ADC clock rate is shown in Figure 9. To reduce the steady state power consumption and to separate the chip’s digital processes from the analog sampling, the ADC is only run after a trigger is sent to the chip. Without a trigger, the quiescent power consumption is $\sim 40$ mW per chip, including the locked VCDL sampling at 10.24 GSa/s and the current biases of all the comparators. Initiating the ADC with a clock rate of 1 GHz causes the power draw to increase from 40 mW to 300 mW within a few nanoseconds. To mitigate high-frequency power supply fluctuations when switching on the ADC, several ‘large’ (2 pF) decoupling capacitors were placed on-chip near the ADC. These capacitors, in addition with the close-proximity evaluation board decoupling capacitors ($\sim 0.1\text{-}10 \mu F$), prevent power supply transients from impairing chip performance.

At the maximum PSEC4 sustained trigger rate of 50 kHz, in which the ADC is running 20% of the time, a maximum average power of 100 mW is drawn per chip.

### 3.5. Frequency Response

The target analog bandwidth for the PSEC4 design was $\geq 1$ GHz. The bandwidth is limited by the...
parasitic input capacitance ($C_{in}$), which drops the input impedance at high frequencies\(^6\) as

$$|Z_{in}| = \frac{R_{term}}{\sqrt{1 + \omega^2 R_{term} C_{in}}}$$  \hspace{1cm} (2)

where $R_{term}$ is an external 50 Ω termination resistor. Accordingly, the expected half-power band-

width is given by:

$$f_{3dB} = \frac{1}{2\pi R_{term} C_{in}}$$  \hspace{1cm} (3)

The extracted $C_{in}$ from post-layout studies was \(~2\) pF, projecting a \(-3\) dB bandwidth of 1.5 GHz which corresponds to the measured value shown in Figure 10. The chip package-to-die bondwire inductance gives a resonance in the response above 1 GHz that distorts signal content at these frequencies. An external filter may be added to flatten the response.

The measured channel-to-channel crosstalk is \(-25\) dB below 1 GHz for all channels as shown in Figure 11. For frequencies less than 700 MHz, this drops to better than \(-40\) dB. The primary crosstalk mechanism is thought to be the mutual inductance between signal bondwires in the chip package. High frequency substrate coupling on the chip or crosstalk between input traces on the PSEC4 evaluation board may also contribute.

3.6. Sampling Calibration

For precision waveform feature extraction, both the overall time-base of the VCDL and the cell-to-cell time step variations must be calibrated. With the rate-locking DLL, the overall PSEC4 sampling time base is stably servo-controlled at a default rate of 10.24 GSa/s. The time-base calibration of the individual 256 delay stages, which vary due to cell-to-cell transistor size mismatches in the VCDL, is the next task. Since this is a fixed-pattern variation, the time-base calibration is typically a one-time measurement.

The brute force ‘zero-crossing’ time-base calibration method is employed [24]. This technique counts the number of times a sine wave input crosses zero voltage at each sample cell. With enough statistics, the corrected time per cell is extracted from the number of zero-crossings ($N_{zeros}$) using

$$<\Delta t> = \frac{T_{input} <N_{zeros}>}{2 N_{events}}$$  \hspace{1cm} (4)

Figure 10: The PSEC4 frequency response. The \(-3\) dB analog bandwidth is 1.5 GHz. The positive resonance above 1 GHz is due to bondwire inductance of the signal wires in the chip package. Similar responses are shown for large and small sinusoidal inputs.

Figure 11: The channel-to-channel crosstalk as a function of frequency. Channel 3 was driven with a \(-2\) dBm sinusoidal input. Adjacent channels see a maximum of \(-20\) dB crosstalk at 1.1 GHz. The electronic noise floor is \(-50\) dB for reference.

\(^6\)This ignores negligible contributions to the impedance due to the sampling cell input coupling. The write switch on-resistance ($\leq 4$ kΩ over the full dynamic range) and the 20 fF sampling capacitance introduce a pole at $\geq 2$ GHz.
where $T_{\text{input}}$ is the period of the input and $N_{\text{events}}$ is the number of digitized sine waveforms. A typical PSEC4 time-base calibration uses $10^5$ recorded events of 400 MHz sinusoids.

The variation of the time-base sampling steps is $\sim 13\%$ as shown in the left plot of Figure 12. Due to a relatively large time step at the first cell, the average sampling rate over the remaining VCDL cells is 10.4 GSa/s, slightly higher than the nominal rate.

The non-linearity of the PSEC4 time-base is shown in the right plot of Figure 12. Each bin in the plot is indicative of the time-base step between the binned cell and its preceding neighbor cell. The relatively large DNL in the first bin, which corresponds to the delay between the last (cell 256) and first sample cells, is caused by a fixed DLL latency when wrapping the sampling from the last cell to the first.

A digitized 400 MHz sine wave is shown in Figure 13 after applying the time-base calibration constants.
3.7. Waveform Timing

The effective timing resolution of a single measurement is calculated by waveform feature extraction after linearity and time-base calibration. A 0.5 Vpp, 1.25 ns FWHM Gaussian pulse was created using a 10 GSa/s arbitrary waveform generator (Tektronix AWG5104). The output of the AWG was sent to 2 channels of the ASIC using a broadband-RF 50/50 splitter (Mini-Circuits ZFRSC-42). This pulse, as recorded by a channel of PSEC4, is shown on the left in Figure 14.

A least-squares Gaussian functional fit is performed to the leading edge of the pulse. The pulse times from both channels are extracted from the fit and are subtracted on an event-by-event basis. A 2-channel RMS timing resolution of 2.6 ps is found as shown on the right in Figure 14.

3.8. Performance Summary

The performance and key architecture parameters of PSEC4 are summarized in Table 1.

4. Application to Large-Area Photodetectors

The first application of PSEC4 is the front-end waveform digitization of large-area photodetectors with picosecond-level time resolution [25, 26]. The LAPPD MCP-PMT is a 20×20 cm$^2$ (8×8 in$^2$) hermetically packaged photodetector with a 30 channel RF microstrip anode signal pick-off [27]. The 1-dimensional transmission line anode design is optimized for precise spatial resolution with an efficient use of electronics channels. The (x,y) position of the incident particle or photon is extracted by using the differential times of waveforms at the two microstrip terminals (x), and the relative charge captured on neighboring strips (y) [27]. Waveform sampling, matched to the MCP bandwidth, allows for both the time and charge extraction to determine the (x,y) position, in addition to the time-of-arrival and energy of the incident particle or photon.

A compact, detector integrated data acquisition (DAQ) system was designed for the LAPPD MCP-PMTs. The front-end microstrip anode waveform digitization board shown in Figure 15, in which five
Table 1: PSEC4 architecture parameters and measured performance results.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>6</td>
<td>die size constraint</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>4-15 GSa/s</td>
<td>servo-locked on-chip</td>
</tr>
<tr>
<td>Samples/channel</td>
<td>256</td>
<td>25 ns recording window at 10.24 GSa/s</td>
</tr>
<tr>
<td>Analog Bandwidth</td>
<td>1.6 GHz</td>
<td>~2.5 dB distortion at 1.3 GHz</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>7%</td>
<td>max. Adjacent channels at 1.1 GHz</td>
</tr>
<tr>
<td>Noise</td>
<td>700 µV</td>
<td>RMS (typical). RF-shielded enclosure.</td>
</tr>
<tr>
<td>Effective ADC Resolution</td>
<td>10.5 bits</td>
<td>12 bits logged</td>
</tr>
<tr>
<td>ADC time</td>
<td>4 µs</td>
<td>max. 12 bits logged at 1 GHz clock speed</td>
</tr>
<tr>
<td>ADC clock speed</td>
<td>1.4 GHz</td>
<td>min. 8-bits logged at 1 GHz</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>1 V</td>
<td>max.</td>
</tr>
<tr>
<td>Readout time</td>
<td>0.8n µs</td>
<td>after linearity correction</td>
</tr>
<tr>
<td>Sustained Trigger Rate</td>
<td>50 kHz</td>
<td>n is number of 64-cell blocks to read (n = 24 for entire chip)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>100 mW</td>
<td>max. per chip. Limited by [ADC time + Readout time]^{−1}</td>
</tr>
<tr>
<td>Core Voltage</td>
<td>1.2 V</td>
<td>0.13 µm CMOS standard</td>
</tr>
</tbody>
</table>

Figure 15: The initial PSEC4 application: a high-channel density waveform digitization of a large-area Micro-Channel Plate (MCP) RF microstrip anode. The two readout boards use five PSEC4 ASICs each to digitize 30 anode strips at both terminals. The active area of the central detector is 20×20 cm².
PSEC4 ASICS are used on each end to capture waveforms from all 30 strips. The board maintains a 50 Ω impedance between the anode output and the chip input. The back-end FPGA and clock-distribution boards (not shown) can be mechanically mounted behind the LAPPD MCP-PMT.

The ‘single-tile’ readout configuration is shown in Figure 15. Depending on the event rate of the application, the detector active area may be increased by serially connecting the microstrip anodes of adjacent LAPPD MCP tiles using a common front-end PSEC4 digitizer board and DAQ system [27].

5. Conclusion

We have described the architecture and performance of the PSEC4 waveform digitizing ASIC. The advantages of implementing waveform sampling IC design in a deeper sub-micron process are shown, with measured sampling rates of 15 GSa/s and analog bandwidths of 1.5 GHz. Potential 0.13 µm design issues, such as leakage and dynamic range, were optimized and provide a 1 V dynamic range with sub-mV electronics noise. A one-time time-base calibration is required to get precise waveform timing with 2-3 picosecond resolution. The first application of the PSEC4 ASIC is the compact, low-power front-end waveform sampling of LAPPD MCP-PMTs.

6. Acknowledgements

We thank Mircea Bogdan, Fukun Tang, Mark Zasowski, and Mary Heintz for their strong support in the Electronics Development Group of the Enrico Fermi Institute. Stefan Ritt, Eric Delagnes, and Dominique Breton provided invaluable guidance and advice on SCA chips. This work is supported by the Department of Energy, Contract No. DE-AC02-06CH11357, and the National Science Foundation, Grant No. PHY-1066014.

References


The Large-Area Picosecond Photo-Detectors Project web page: <http://psec.uchicago.edu>
