DUAL-OUTPUT HOLA
MAY 2011 STATUS

Anton Kapliy
Mel Shochet
Fukun Tang
Take-away message

- Designed a new dual-output HOLA board with independent flow control from DAQ and FTK channels
- Wrote new firmware to interface the S-LINK core to inexpensive Altera Cyclone IV GX transceivers
  - Simulated using a comprehensive Modelsim testbench
- Manufactured, stuffed, and tested two prototype boards:
  - Firmware uploaded to a 4 Mbit serial loader (EPCS4)
  - Sent data through both channels
  - Ensured that flow control can be asserted from either channel
  - Tested bit error rate to 6E13 while reading from both channels
- What remains to be done:
  - Test one board to EBR=1E15 (~21 days for dual-channel test)
  - Move the optical transceiver cages outwards to comply with S-LINK physical size specifications
What is a HOLA?

A device that implements the S-LINK protocol for point-to-point data transfer.

Pixel and SCT data in a ROD is organized into 32-bit chunks and sent to a HOLA card, which serializes and sends it through optical fibers.

Another HOLA card receives this data stream in a ROB (and FTK DF) and de-serializes it.

S-LINK implements data framing, error detection, and flow-control.
FIFO provides a parallel interface to an outside SERDES device (TLK-2501), which feeds serial signal to an optical transmitter.

Note that TLK-2501 alone costs more than the entire FPGA that we are now using and consumes four times as much power!
The original LSC core is slightly modified:

- ALTGX fetches data into the phase comp FIFO using a special clock (TX_CLK), propagated back to the LSC core
- For better metastability protection, 50 MHz clock made related to TX_CLK
- Flow control from FTK
A similar testbench (with two LDC+ROMB receivers) was implemented in Mentor Graphics Modelsim. FEMB, LDC, and ROMB were simulated functionally, while LSC – using a compiled & fitted (i.e. gate-level) Altera Quartus design.

A similar testbench was also set up in hardware using a PC with two PCI slots.
PC setup: ROD side

S32PCI64 “SOLAR” mezzanine card: Provides access to S-LINK via PCI bus

The first prototype of dual-output HOLA

Parallel connector to transfer 32-bit data

2 x optical transceivers

FEMB

S-LINK LSC
PC setup: ROB and FTK side

Identical data is received from the two fibers running from the dual-output HOLA. Note that each channel retains independent flow control.

“FILAR” card (based on S32PCI64):
- Implements S-LINK protocol
- Provides access to S-LINK via PCI bus

The two channels are read out independently. E.g., we can read out all pending buffers from DAQ, so that only FTK will be asserting flow control.

S-LINK LDC and ROMB (in one package)
EBR tests

- We use the so-called SLIDAS mode in SOLAR PCI card
  - Continuously sends frames with 254 words x 32 bits to HOLA LSC
  - Patterns follow a pseudo-random sequence reproducible in C++
    - We can check word-by-word that all received patterns are correct
- PC presents a bottleneck: need to generate these pseudo-random patterns and compare them with all received data words.
  - We can achieve about 65 MB/s (21 days to test EBR to 1E15).
- But it also continuously exercises flow control:
  - FEMB wants to send at nearly 200 MB/s, but ROMB & LDC buffers (~20 KB) quickly fill up and assert flow control until they finish reading out
  - Flow control is asserted / de-asserted continuously during test