Electronics *Development* *for pSec Time-of-Flight Detectors*

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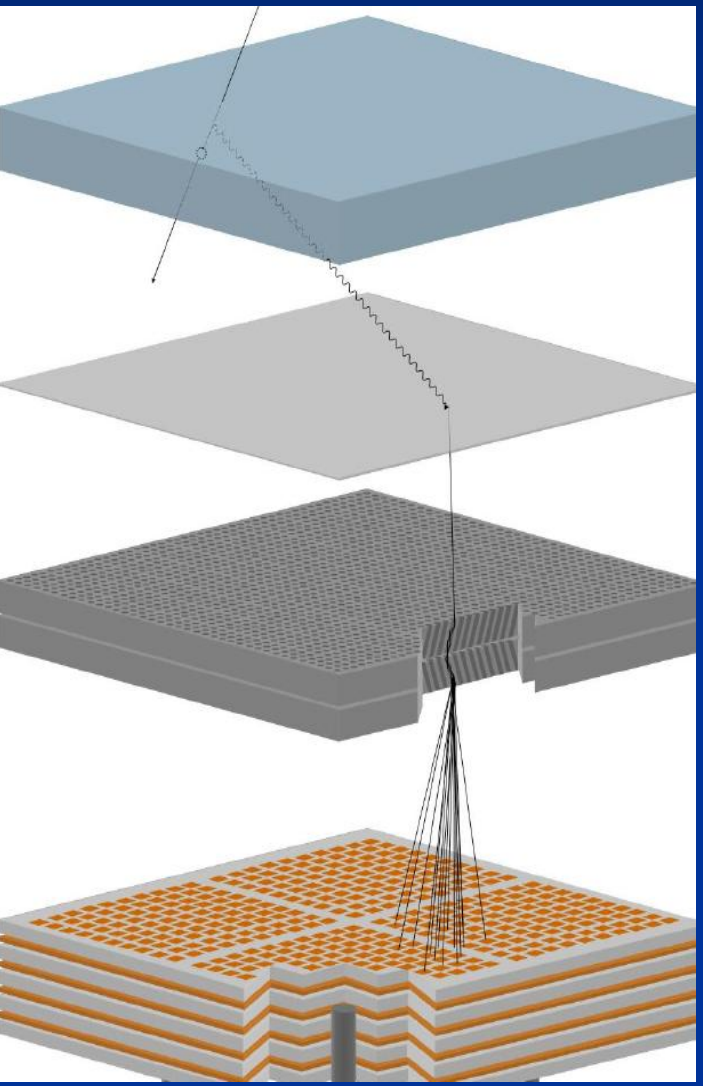
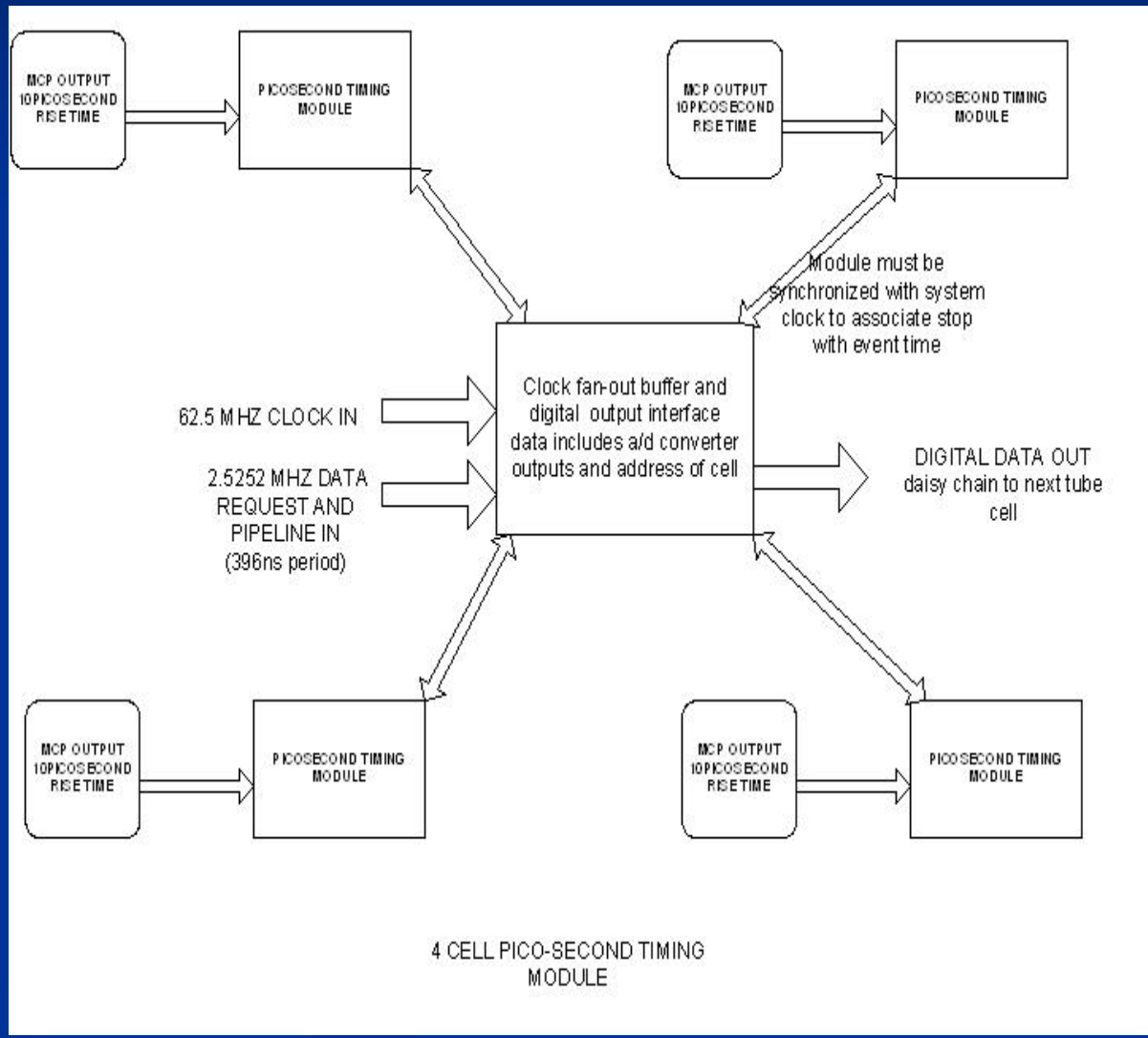
Introduction: Readout Electronics System

Anode structure



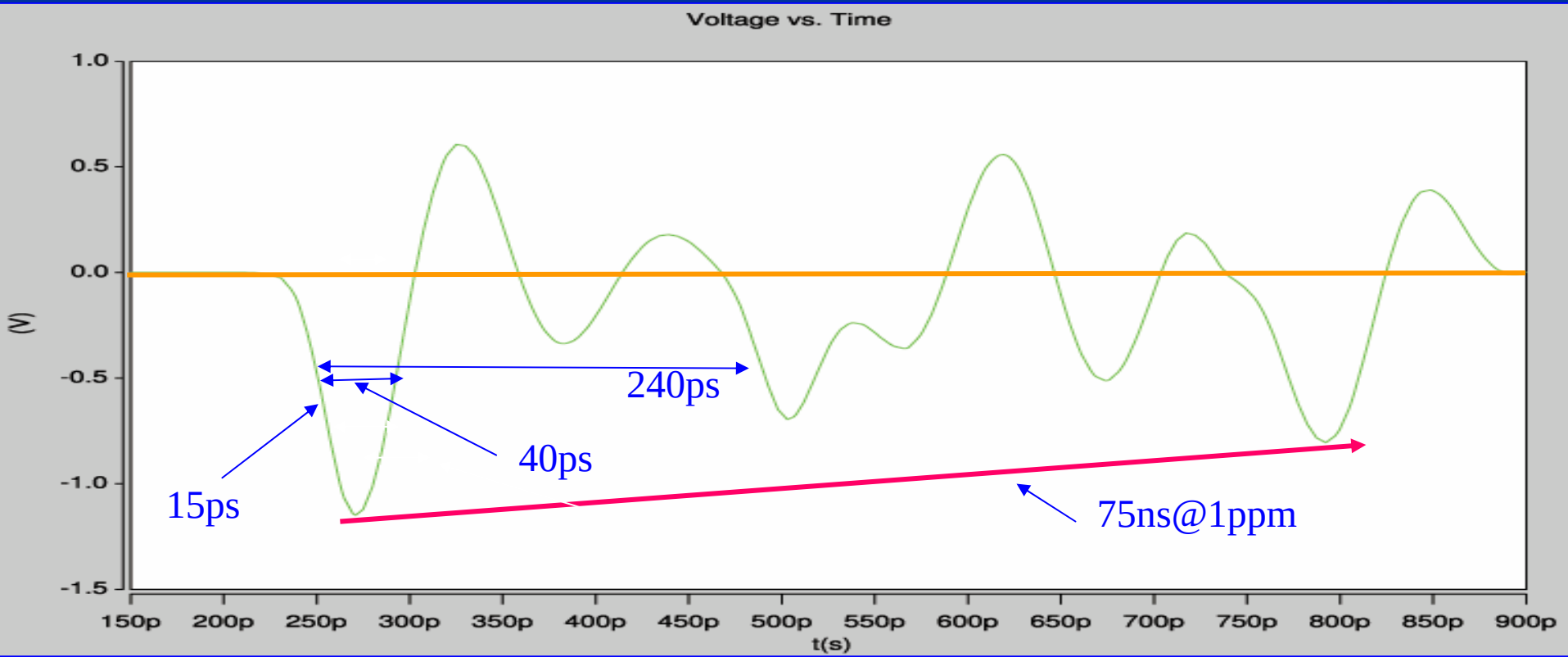
Harold's TOF system



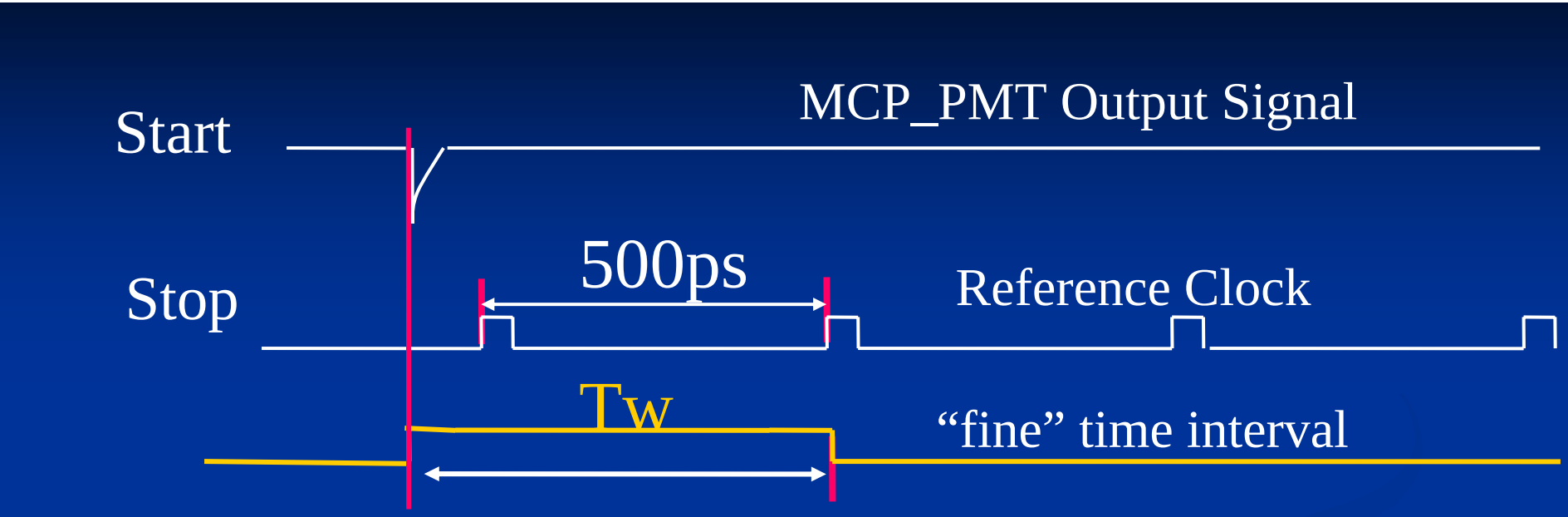
Characteristics of MCP-PMT Output Signal

MCP-PMT output signal from Tim' simulation

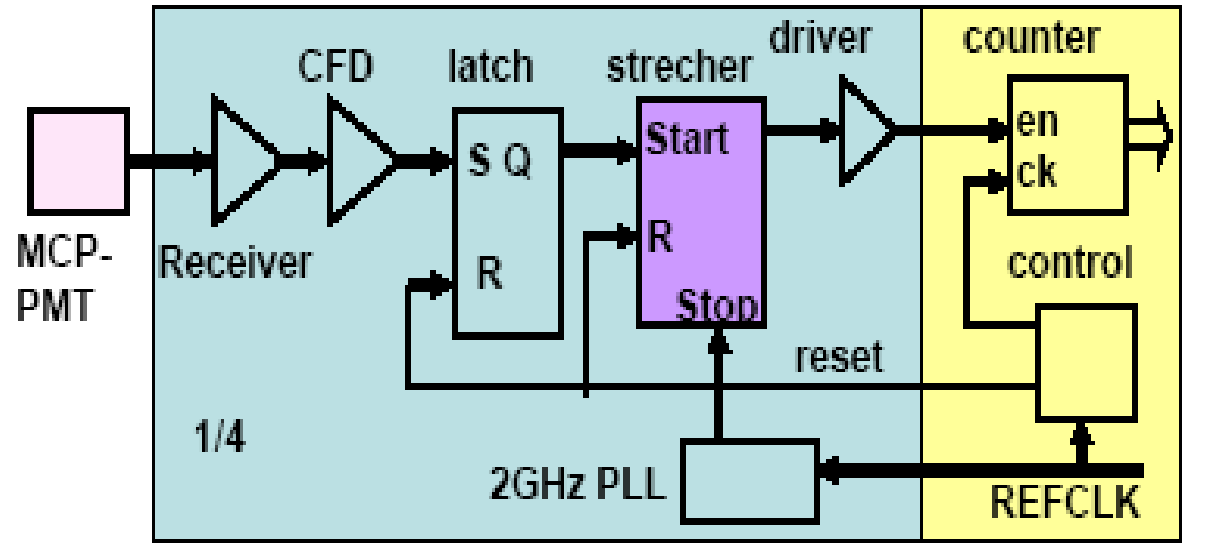
- Rise time 15ps (equivalents to a signal bandwidth of 23.3 GHz)
- Pulse width (FWHM): 40ps
- Reflection coefficient: -0.98 (Load=100 ohms)
- Reflection time delay (round trip): 240ps
- Recovery time: 75ns (Settled at 1ppm)

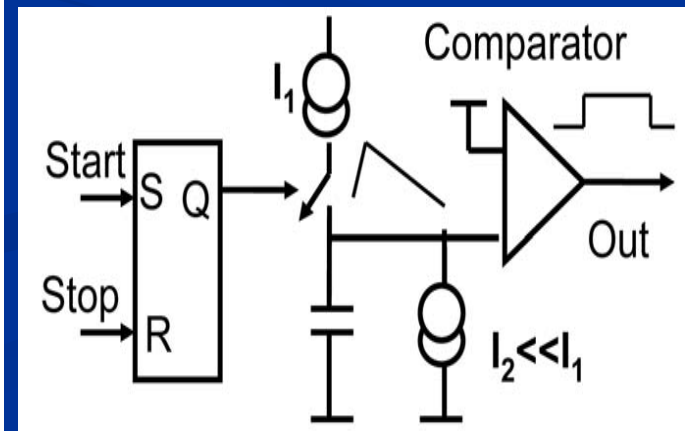


Proposed Time Stretcher TDC with 1ps Resolution



psFront-end





Electronics Requirements & Process Evaluations

Input signal bandwidth:	*~23.3GHz*
Input signal width (FWHM):	*~40ps*
TDC resolution:	*~1ps*

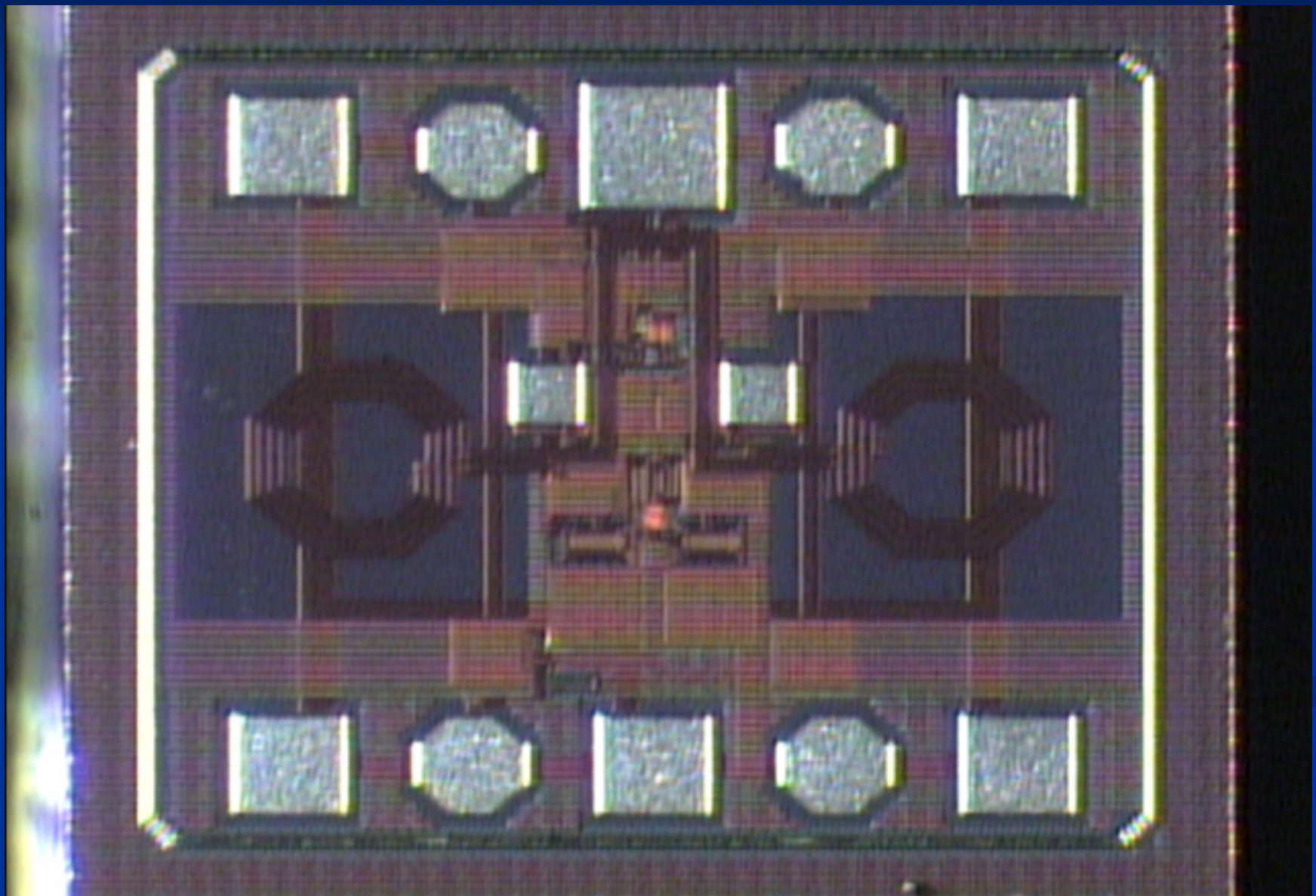
Minimum Requirements:

- ultra low noise, ultra high f_T transistors
  - > 5-10x of the input signal bandwidth ~ *(110-220GHz)*
- stable passive components
  - Inductors, MIM Capacitors, Resistors, Varactors …

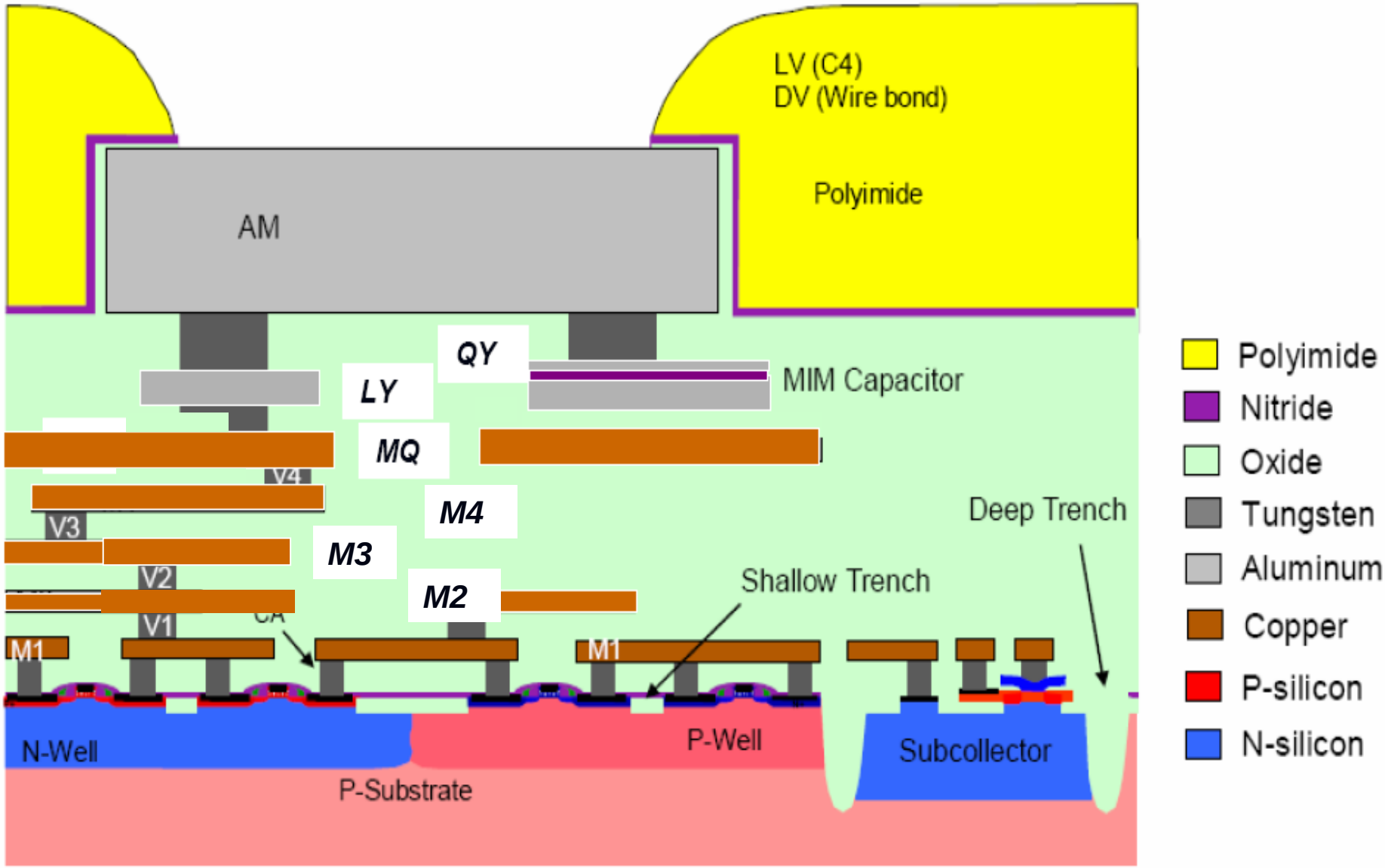
Available Processes:

- IHP SiGe BiCMOS 0.25µm technology:
  (SG25H1, SG25H2) --- *Europractice*
- IBM SiGe BiCMOS 0.13µm Technology:
  (8HP) --- *MOSIS*

UC designed 2 GHz VCO with 55 fsec Cycle-to-Cycle Timing Jitter Using IHP SG25H1 Process



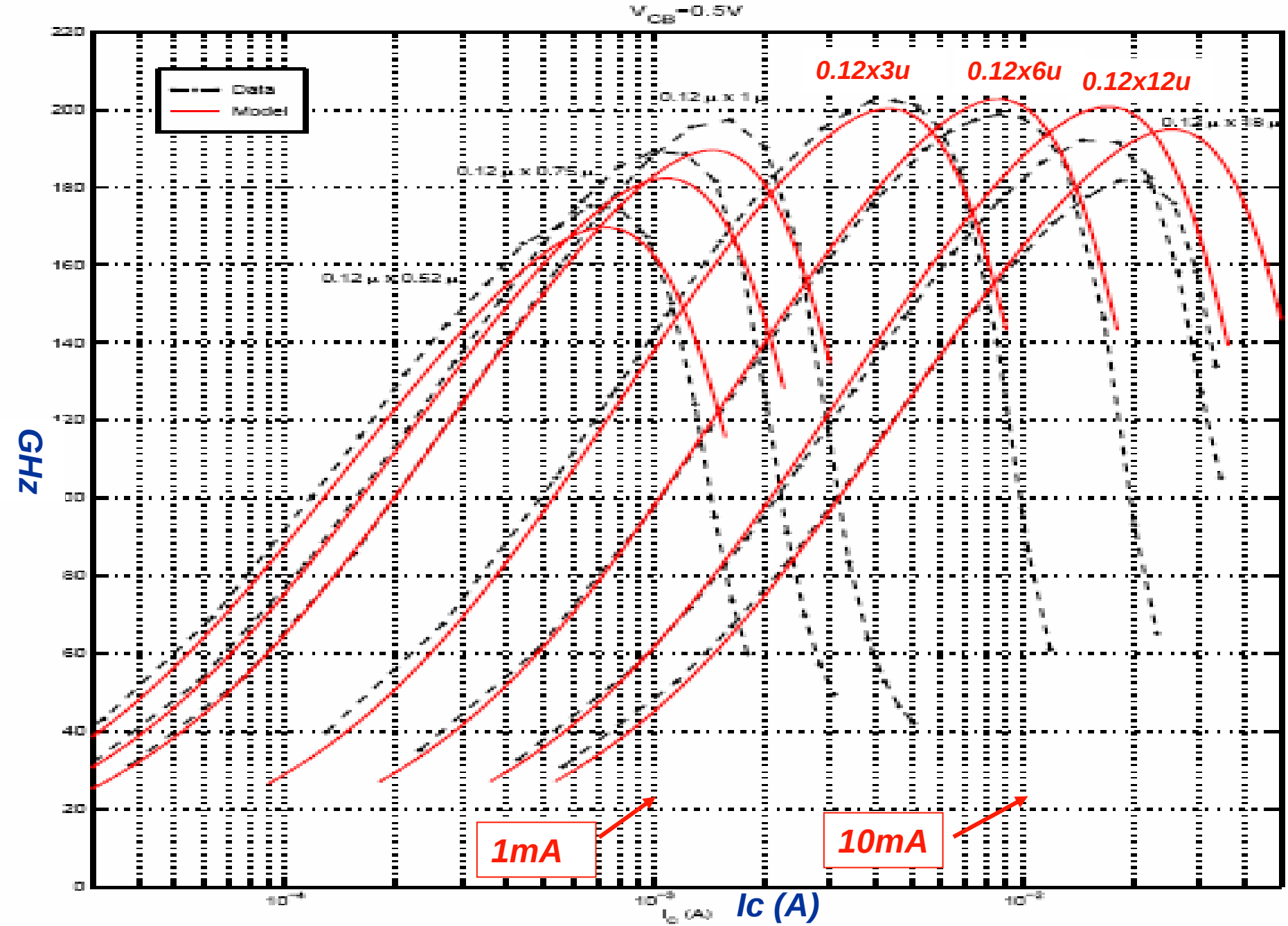
IBM SiGe BiCMOS8HP Process Cross-section



Brief Summary of IBM BiCMOS8HP Process

- SiGe hetero-junction bipolar transistors
  - *f_T (high performance): 200GHz, BVceo=1.7V, BVcbo=5.9V*
  - *f_T (high breakdown): 57GHz, BVceo=3.55V, BVcbo=12V*
- High-Q inductors and metal-insulator-metal capacitors
- 4 types of low-tolerance resistors with low and high sheet resistivity
  - *n+ diffusion, tantalum nitride, p+ polisilicon and p- polisilicon*
- CMOS transistors (VDD=1.2V or 2.5/3.3V)
  - *Twin-well CMOS*
  - *Hyperabrupt junction and MOS varactors*
- Deep trench and shallow trench isolations

8HP NPN Ft Characteristics vs. Emitter size (25C)

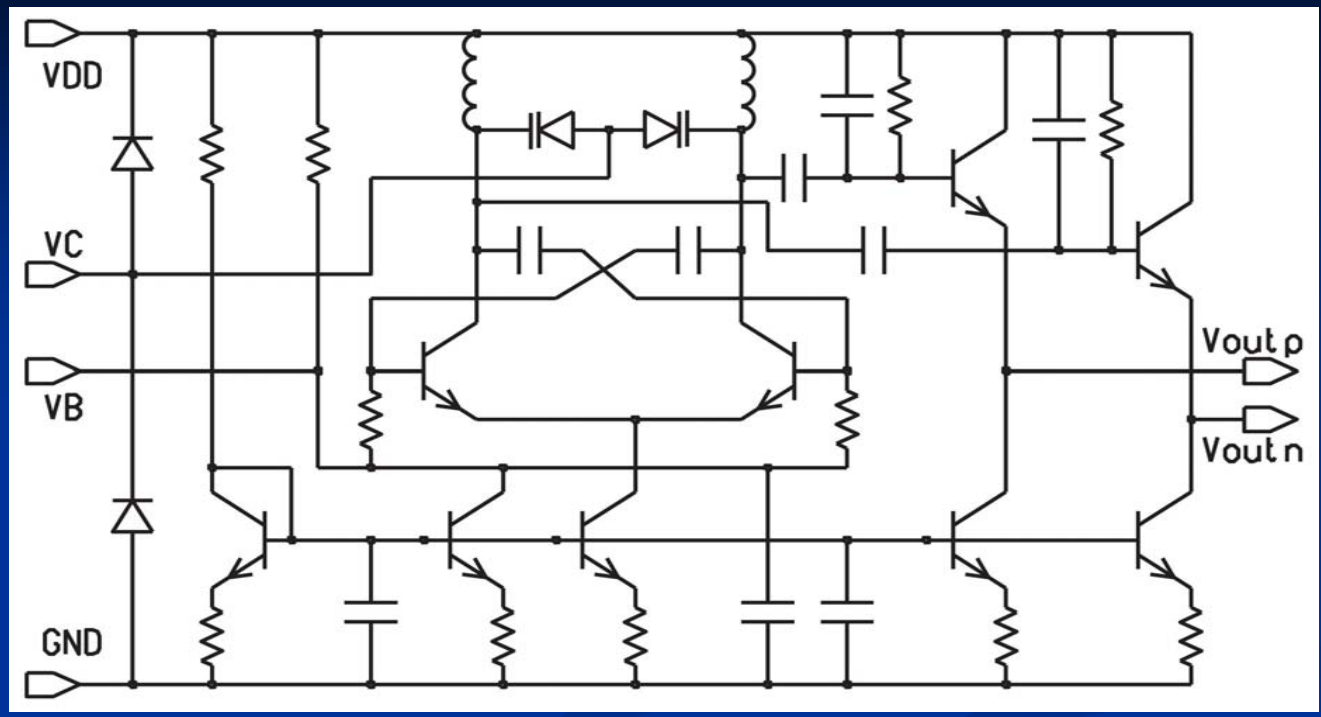


2GHz VCO Design using IBM SiGe BiCMOS8HP Process

EDA Tools:
Cadence Virtuoso Analog Environment

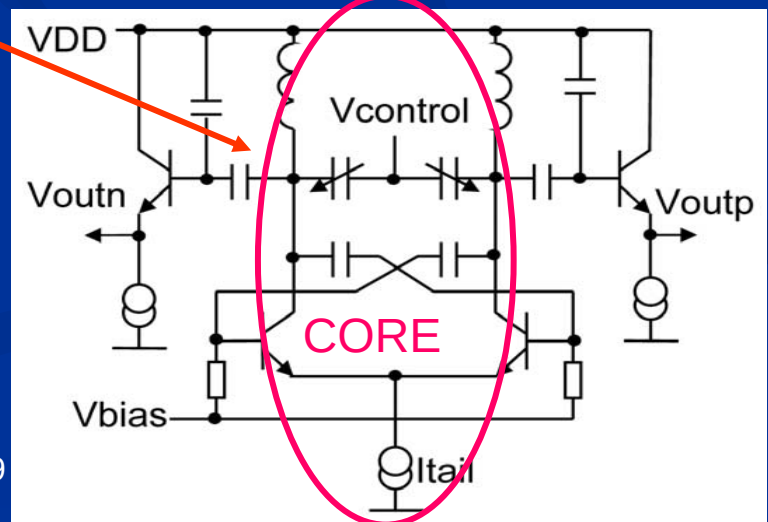
Verification Tools:

Diva/Assura



Simplified VCO Schematic

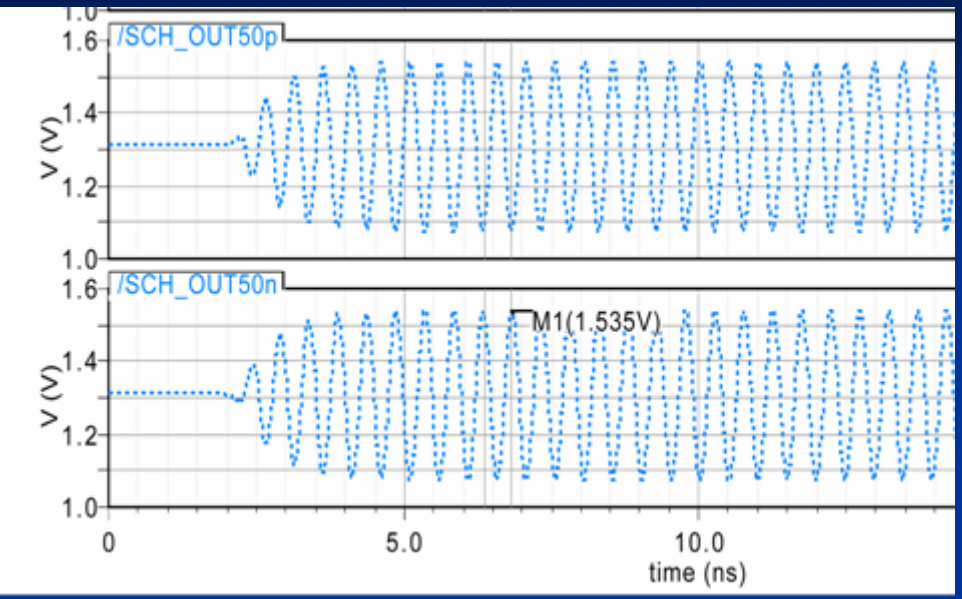
Core

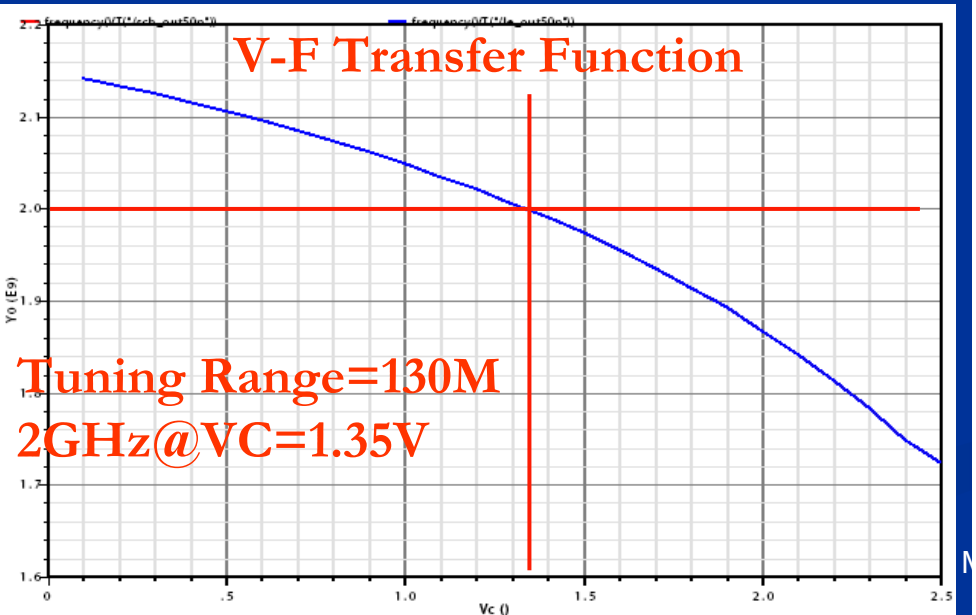


- Purely hetero-junction transistors
- Negative resistance
- On-chip high-Q LC tank
- High Frequency PN diode Varactors
- Capacitor voltage dividers
- 130Mhz tuning range
- Full differential 50-ohm line drivers

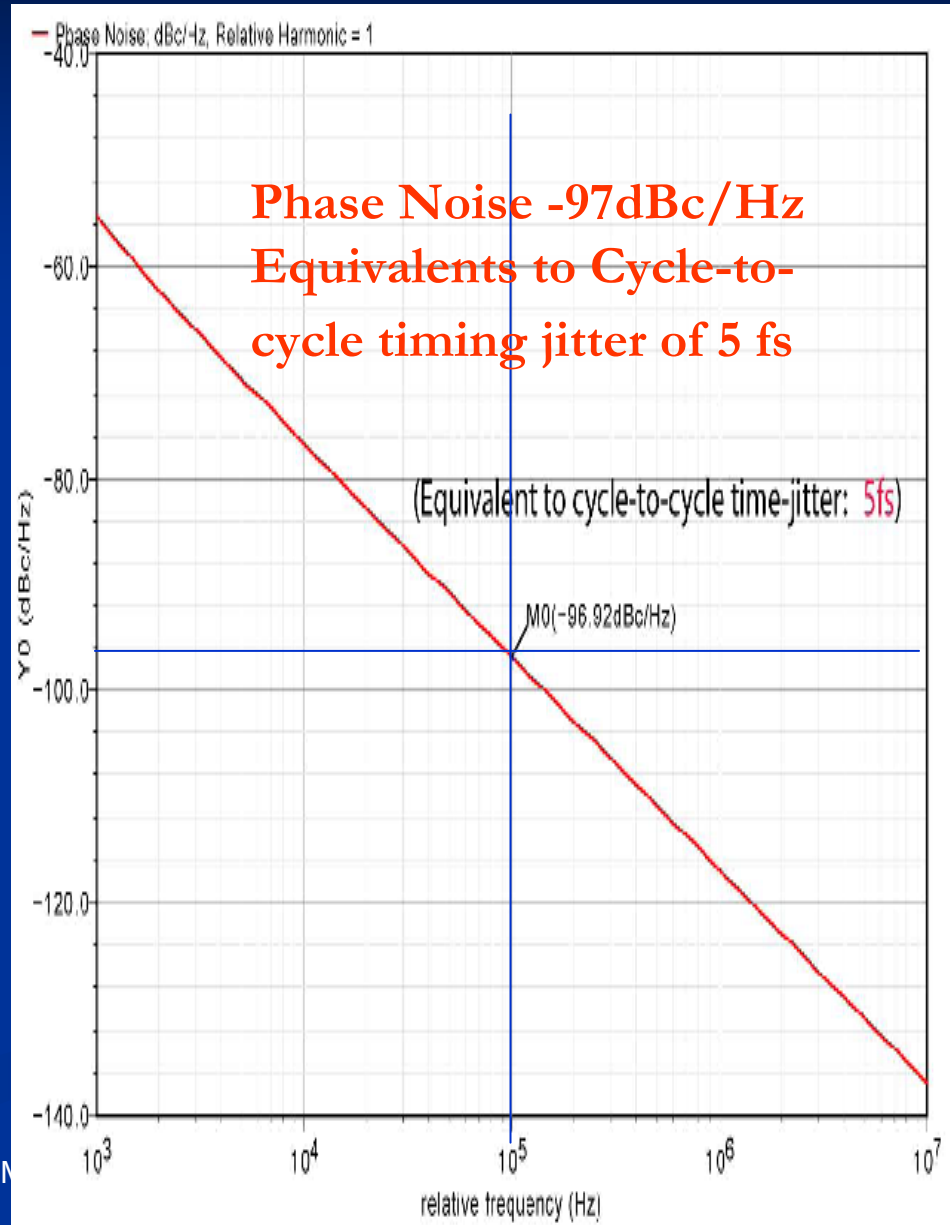
VCO Schematic (Pre-layout) Simulation Result

Transit Outputs





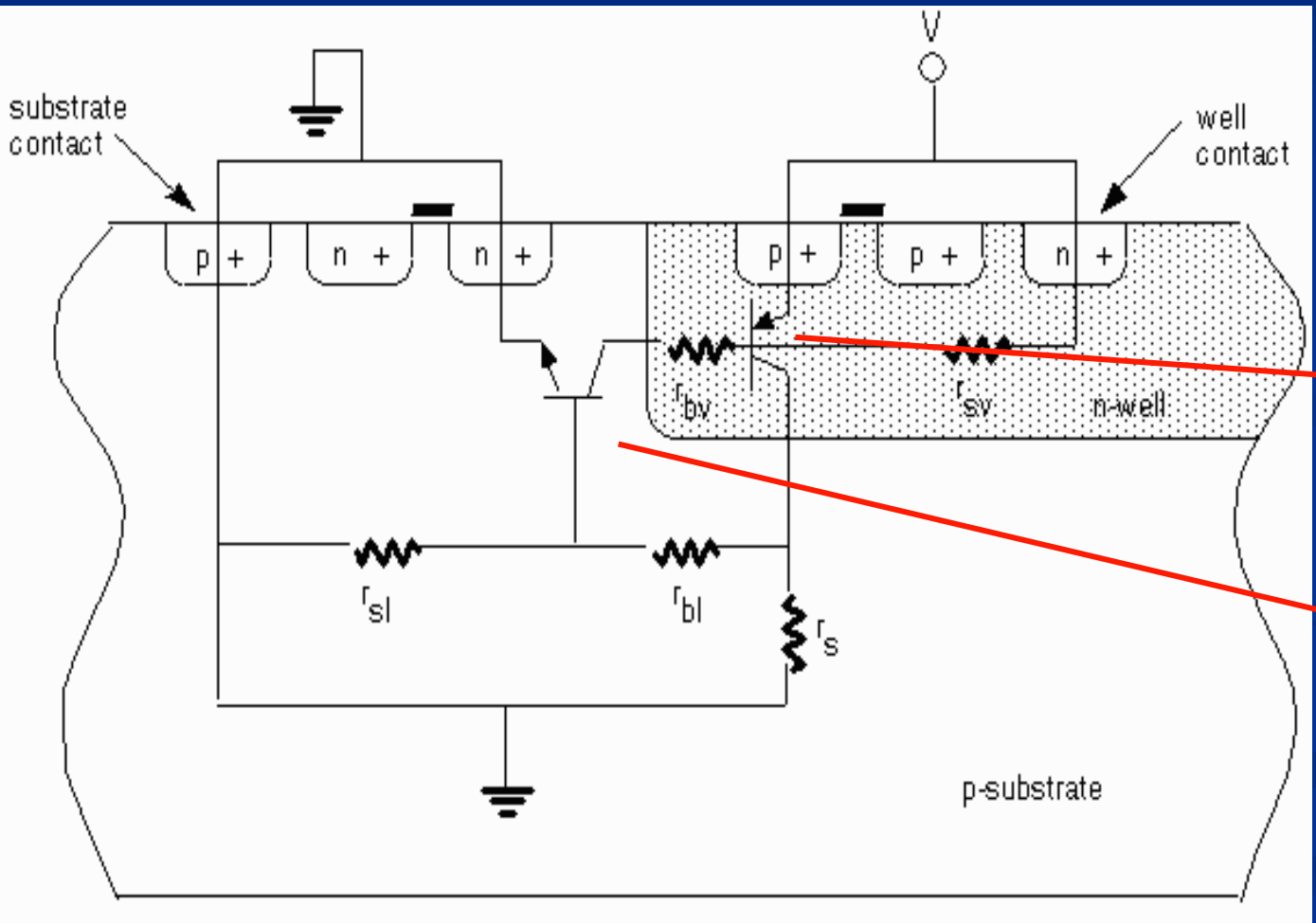
Phase Noise

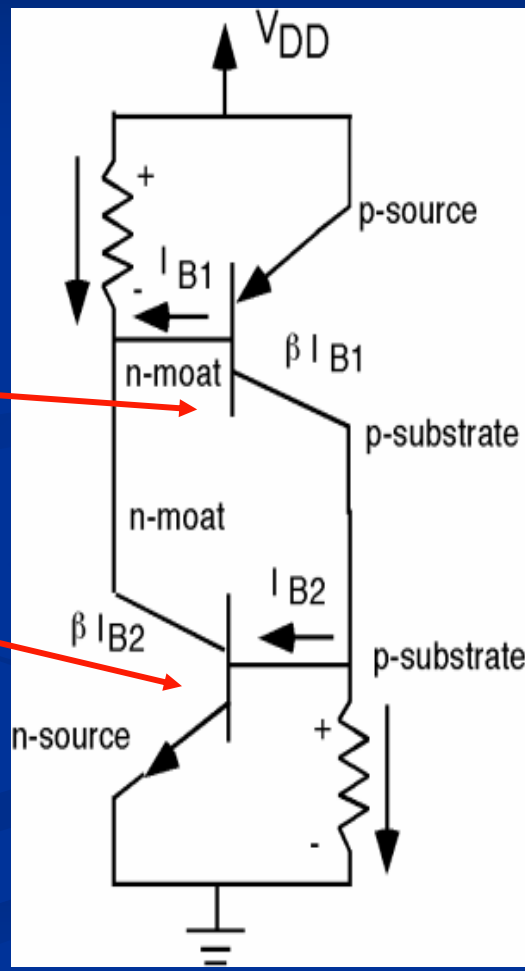


Analysis of CMOS Latchup

Famous CMOS latch-up which created by parasitic lateral pnp and npn transistors

Solution: apply substrate contacts and tie them to the lowest voltage terminals
apply shallow trenches to increase isolation





Substrate Noise Minimization

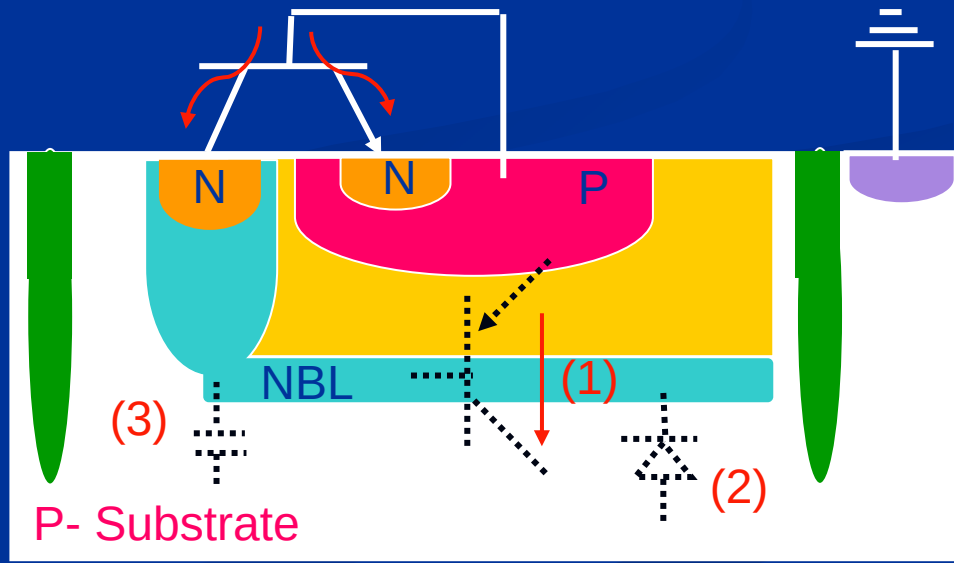
(1) One of the major substrate noise is caused by current injection from bipolar transistors working in saturation mode.
(2) Substrate PN diode occasionally forward biased by EMI interference or some other reasons.
(3) Parasitic coupling capacitance

Solution:

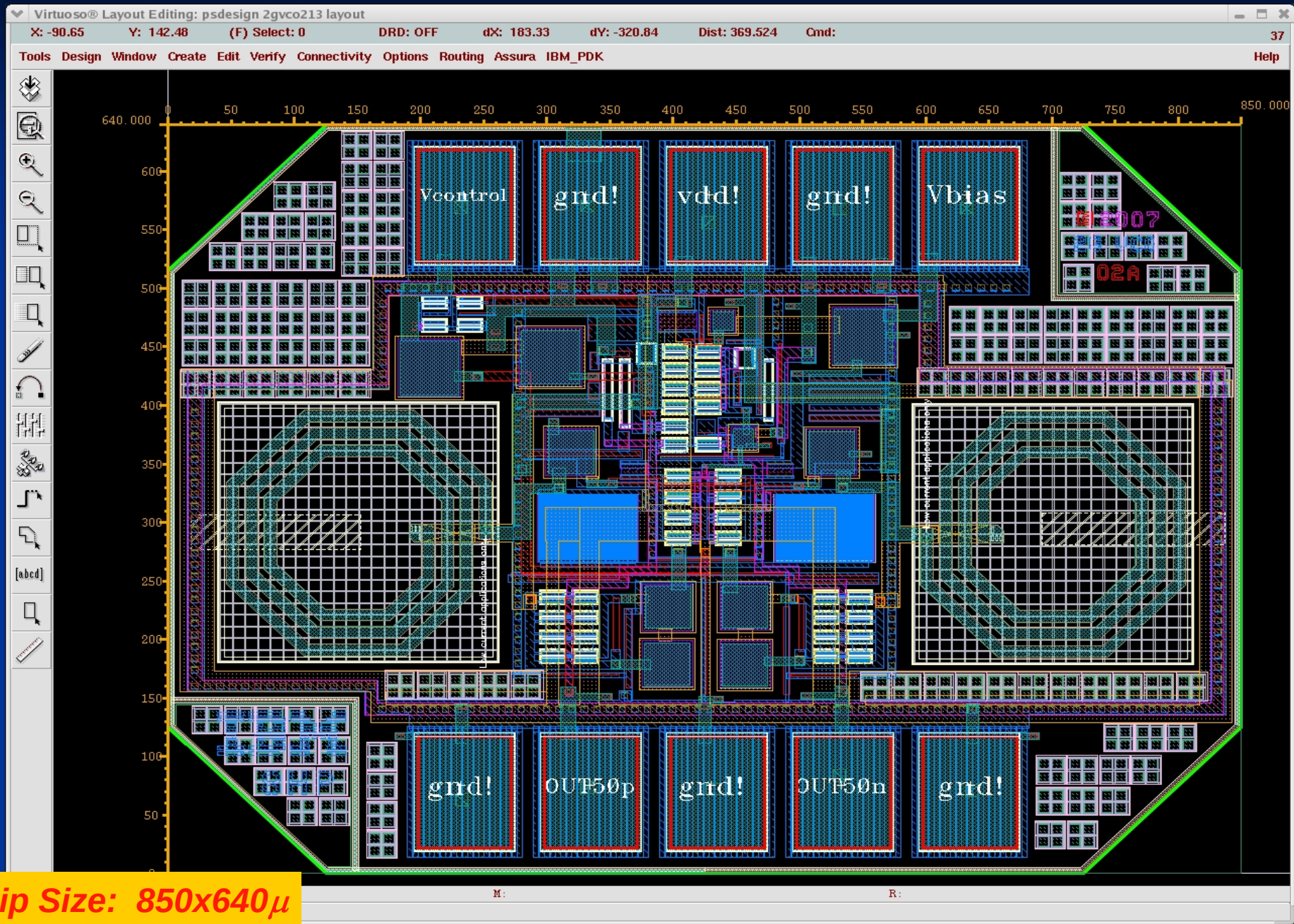
Prevent transistors from working in saturation mode unless you have to.

apply substrate contacts and tie them to the lowest voltage potential on the chip.

apply deep or shallow trench shielding rings to increase isolation



UC Designed 2GHz VCO Chip with 5 fsec Cycle-to-Cycle Time Jitter Using IBM 0.13µm SiGe BiCMOS8HP Process (Feb. 2007)



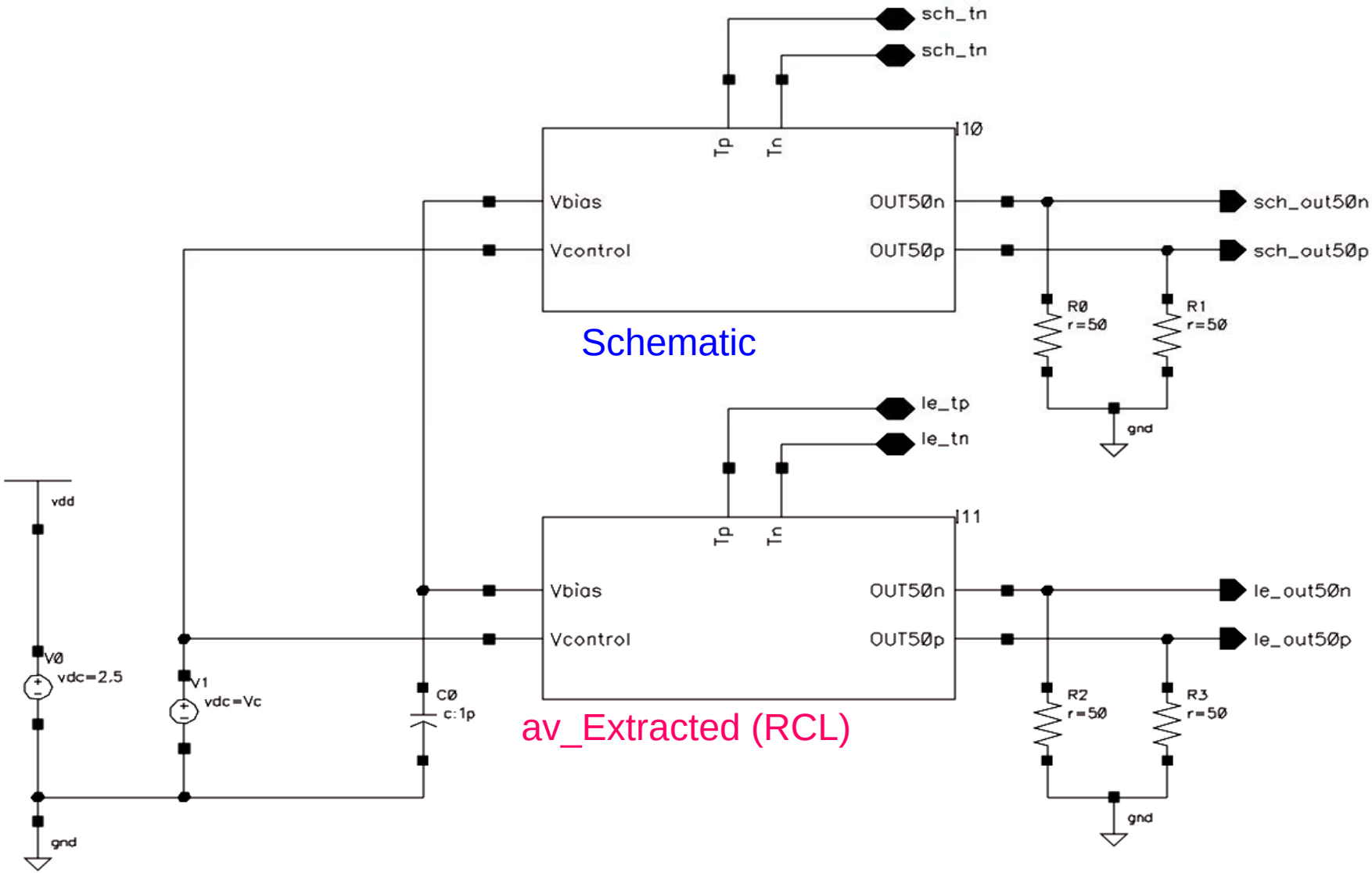
Chip Size: 850x640µ

Layout and Parasitic Extraction

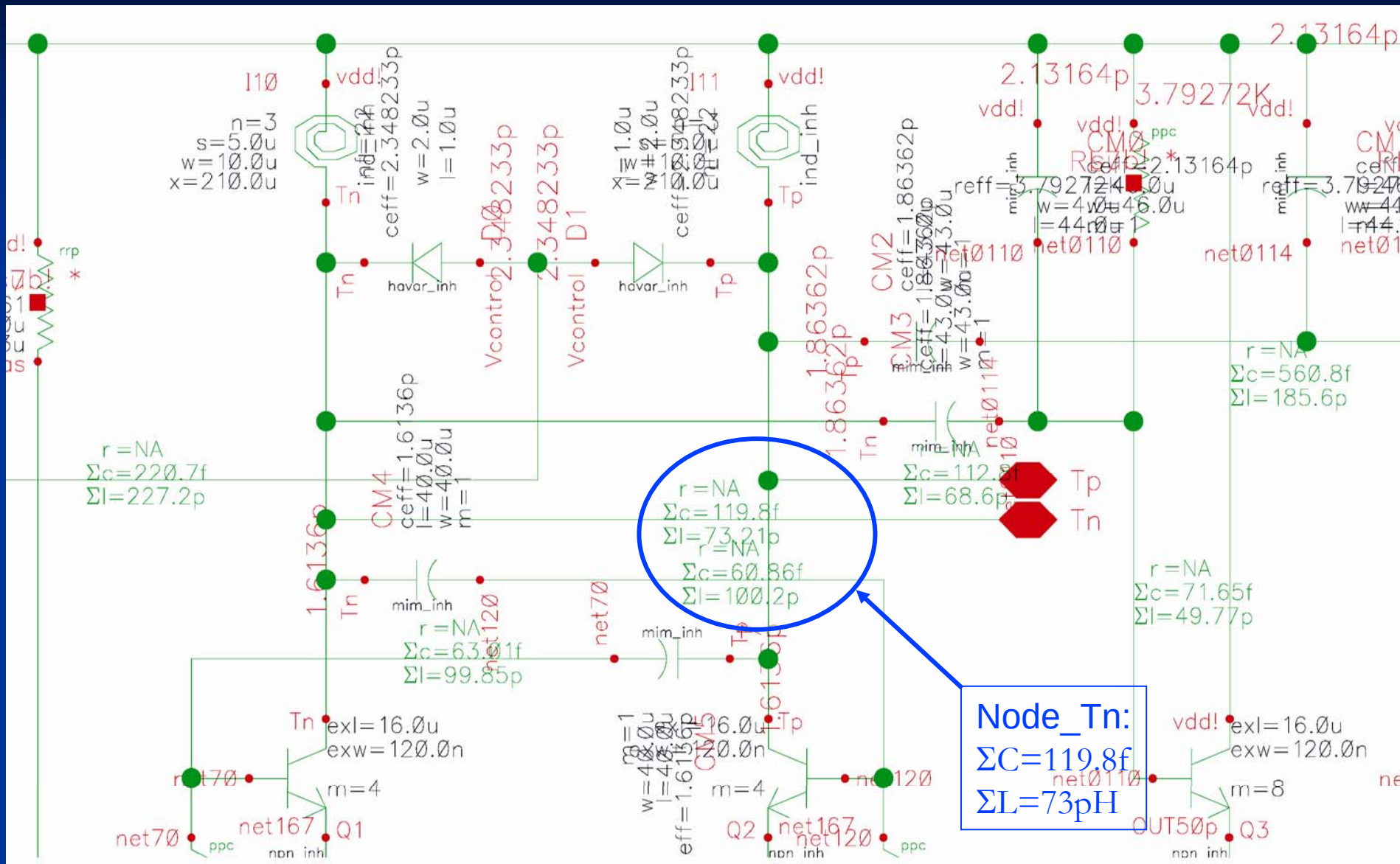
- Diva/Assura DRC Check
- Diva/Assura LVS Check
- Floating Gate, NWell & Antenna Check
- Global Pattern Density Check
- Local Pattern Density Check
- GR594 (Dendrite Rules) Check
- Assura RCL extraction
- GDSII Stream Out (CDS → GDSII mapping)
- GDSII/Layout Comparison Check

Backup your full data after you passed all checks!!!

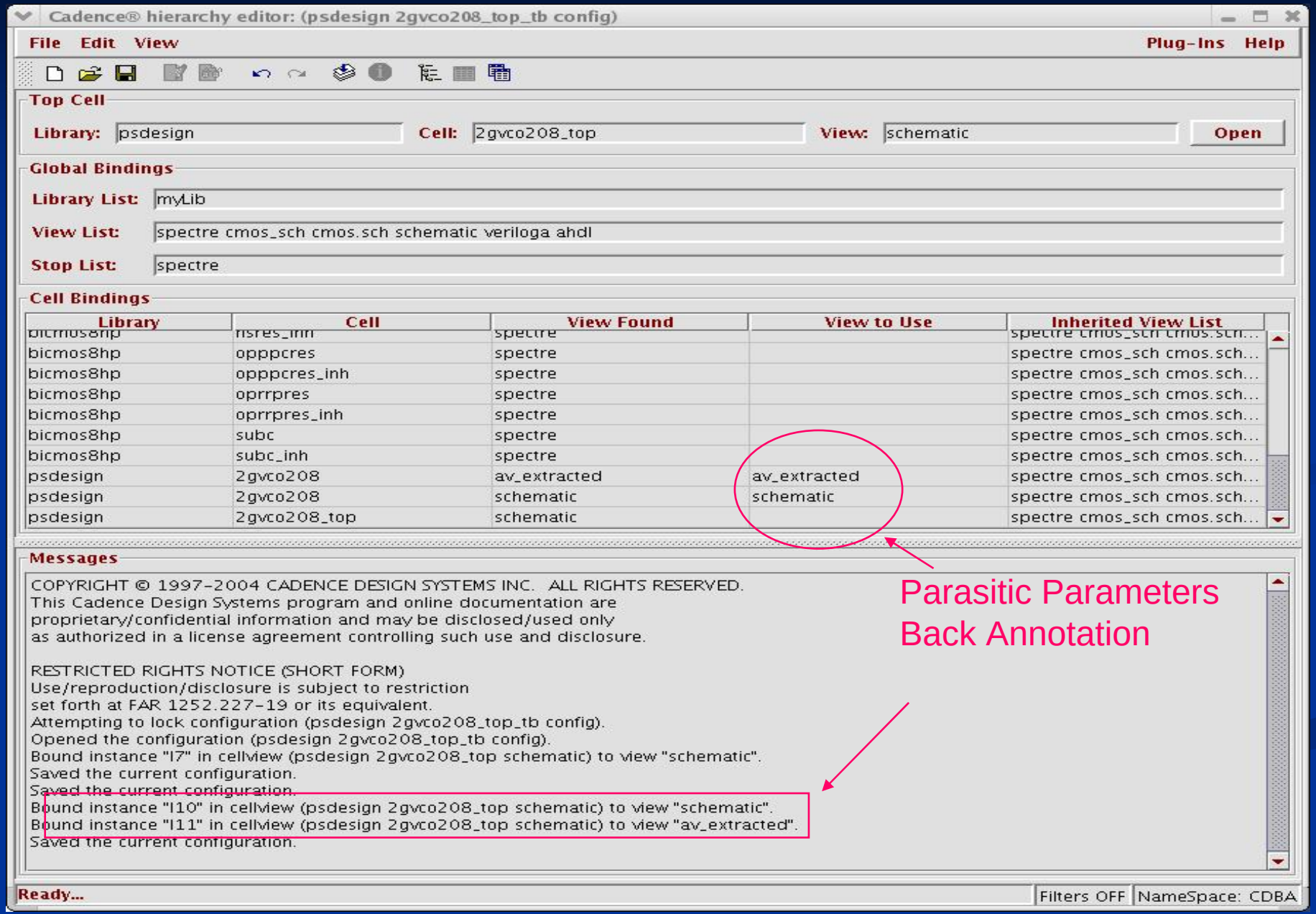
Schematic & Post Layout Comparison: Hierarchy Setup



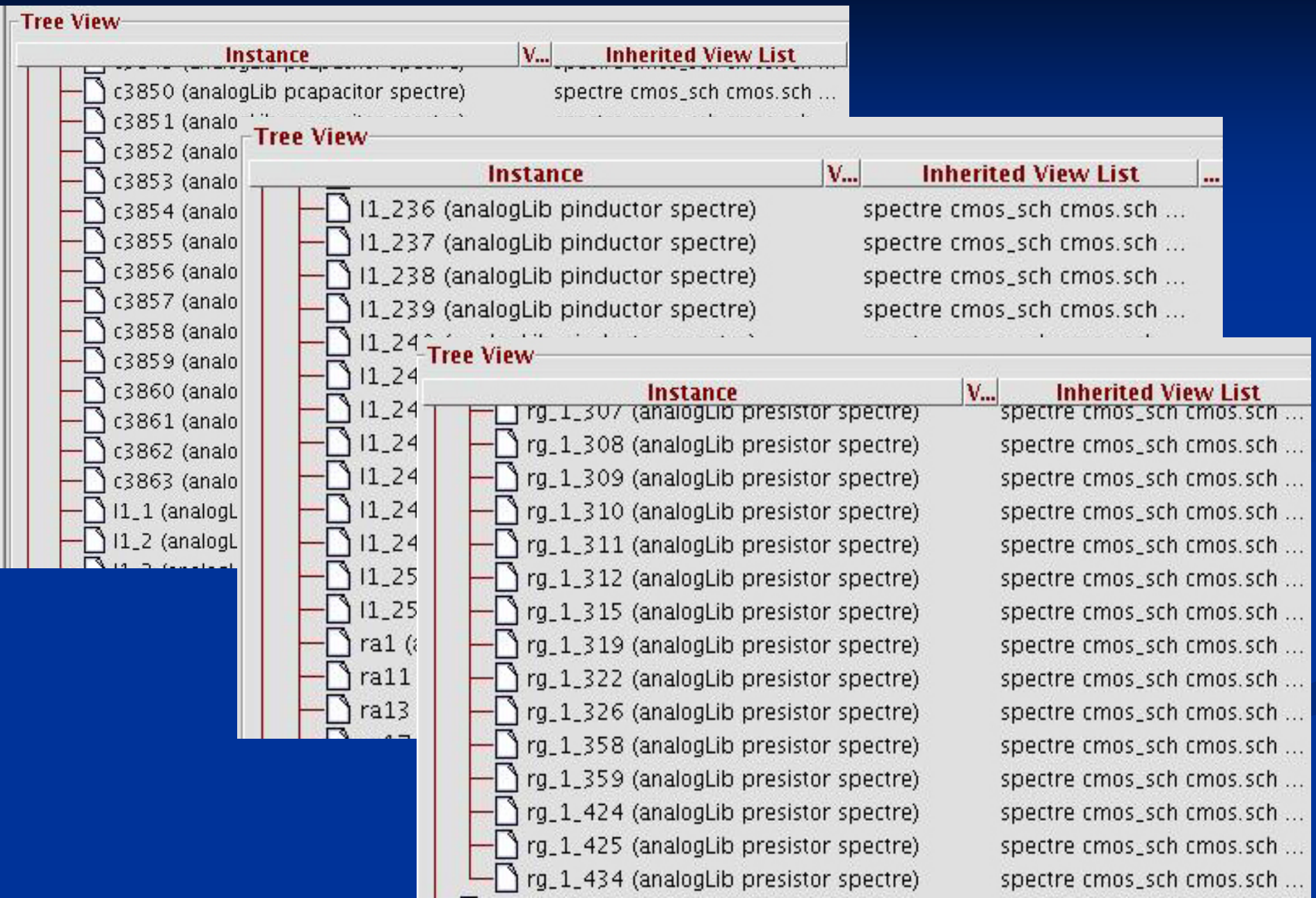
RLC_Extracted Schematic Back Annotation View



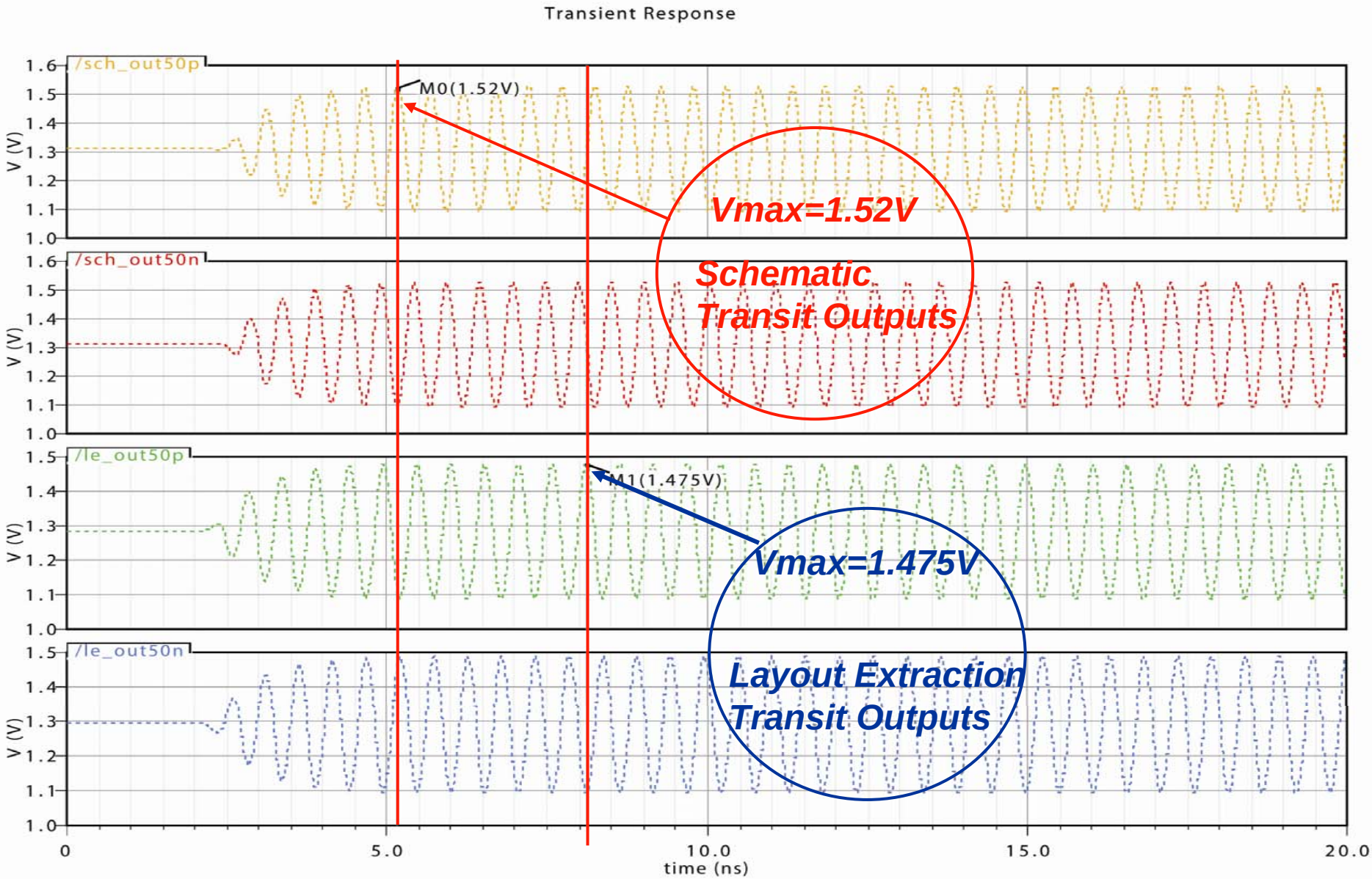
Post Simulation: Configuration Setup



Post Simulation Parasitic Parameter List

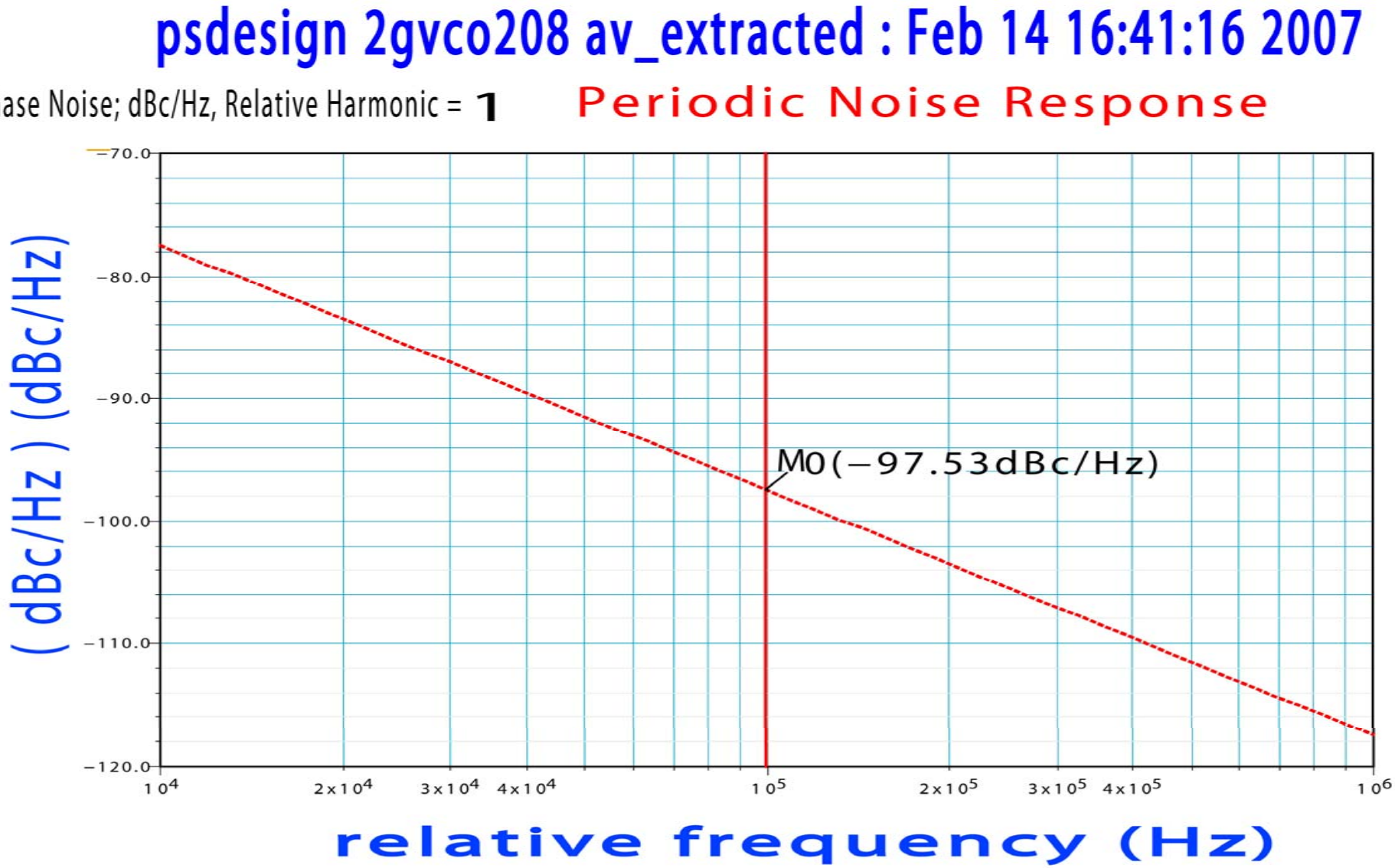


Schematic/Post Layout Simulation Comparison:
Transit Outputs (first layout)



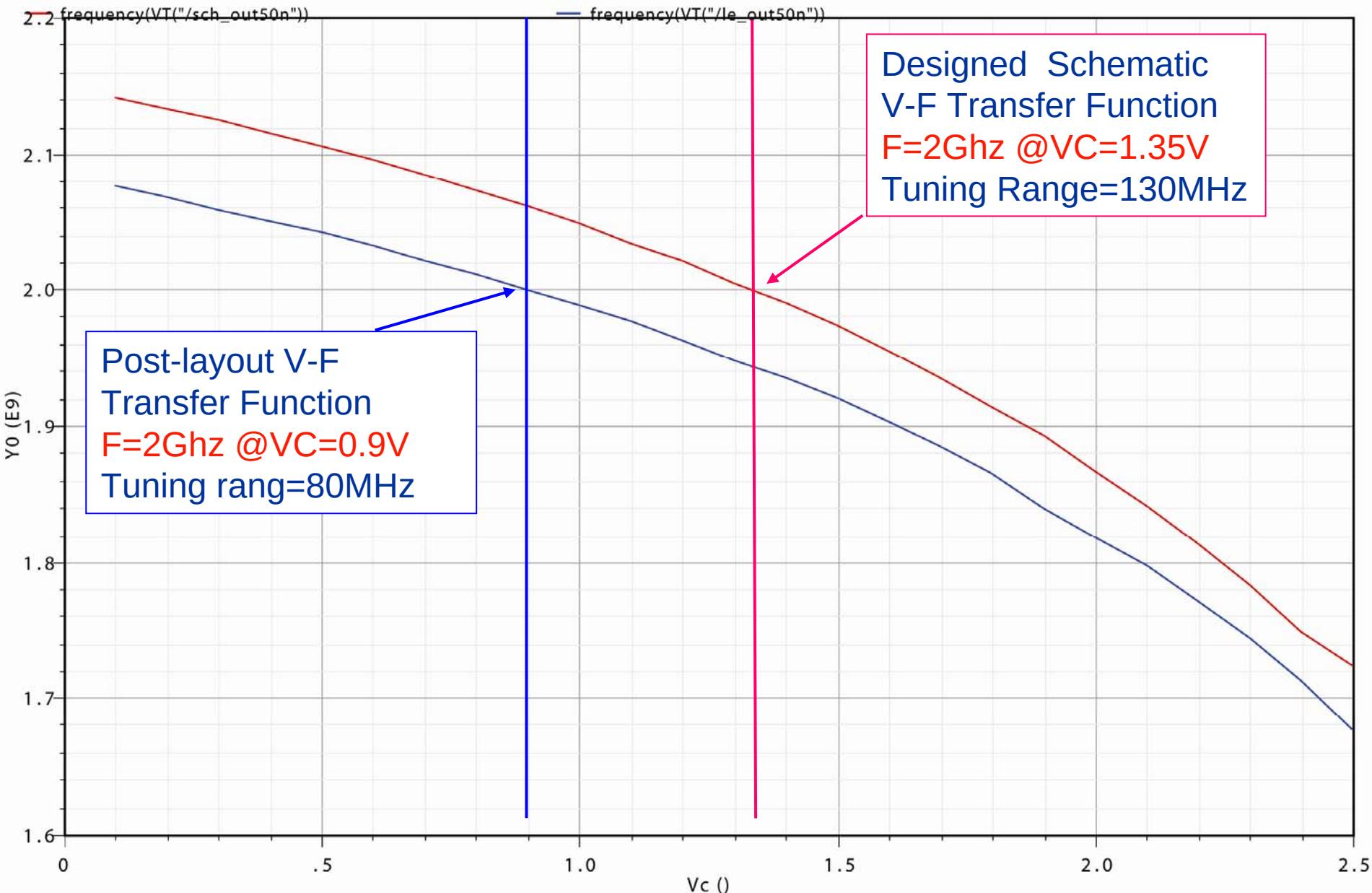
VCO Post Layout Simulation Result (First Layout)

Output Phase Noise Spectra Plot



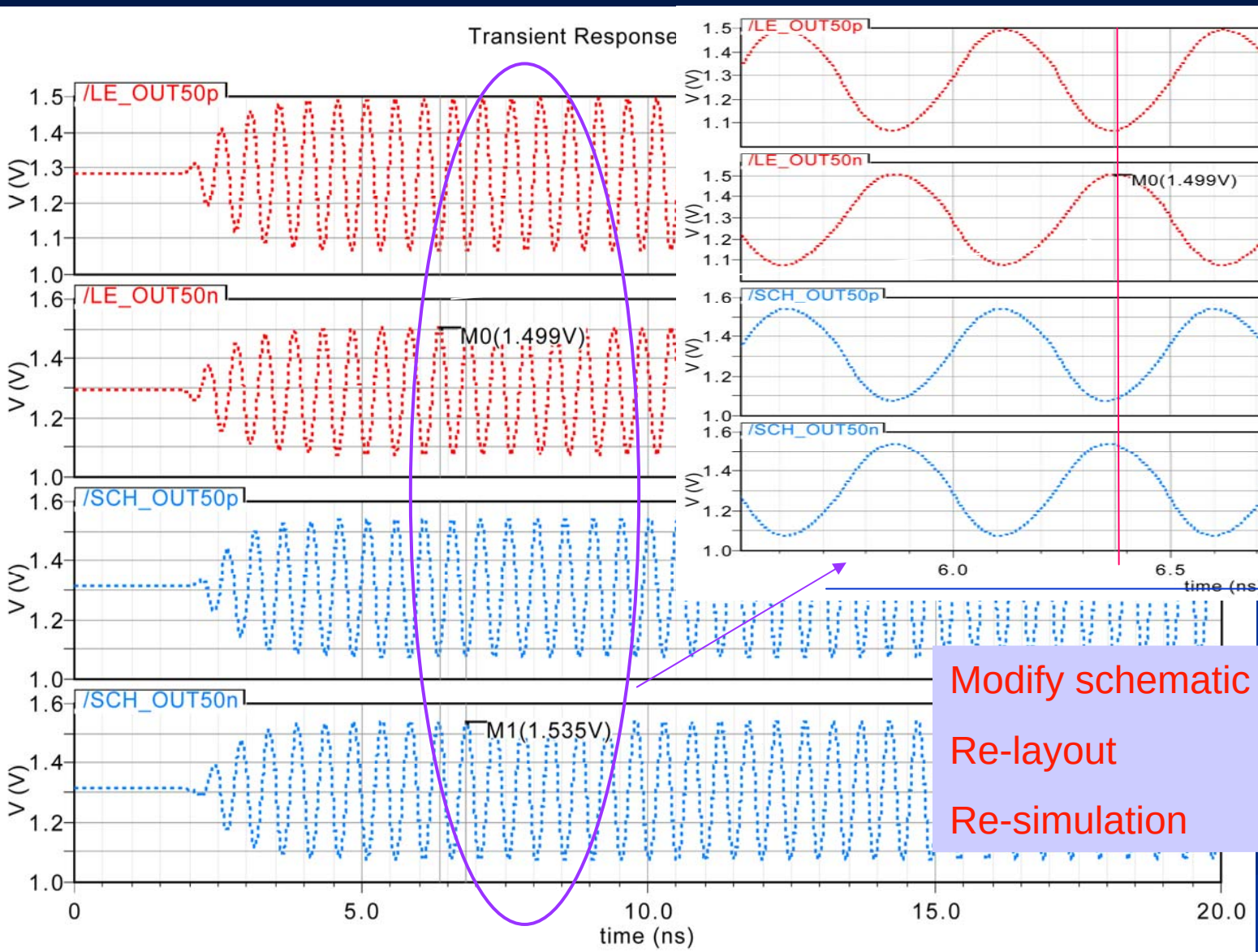
Schematic/Post Layout Simulation Comparison:

V-F Transfer Function Plot (first layout)



VCO Post Layout Transit Simulation Result (Final)

Transit Output Waveforms



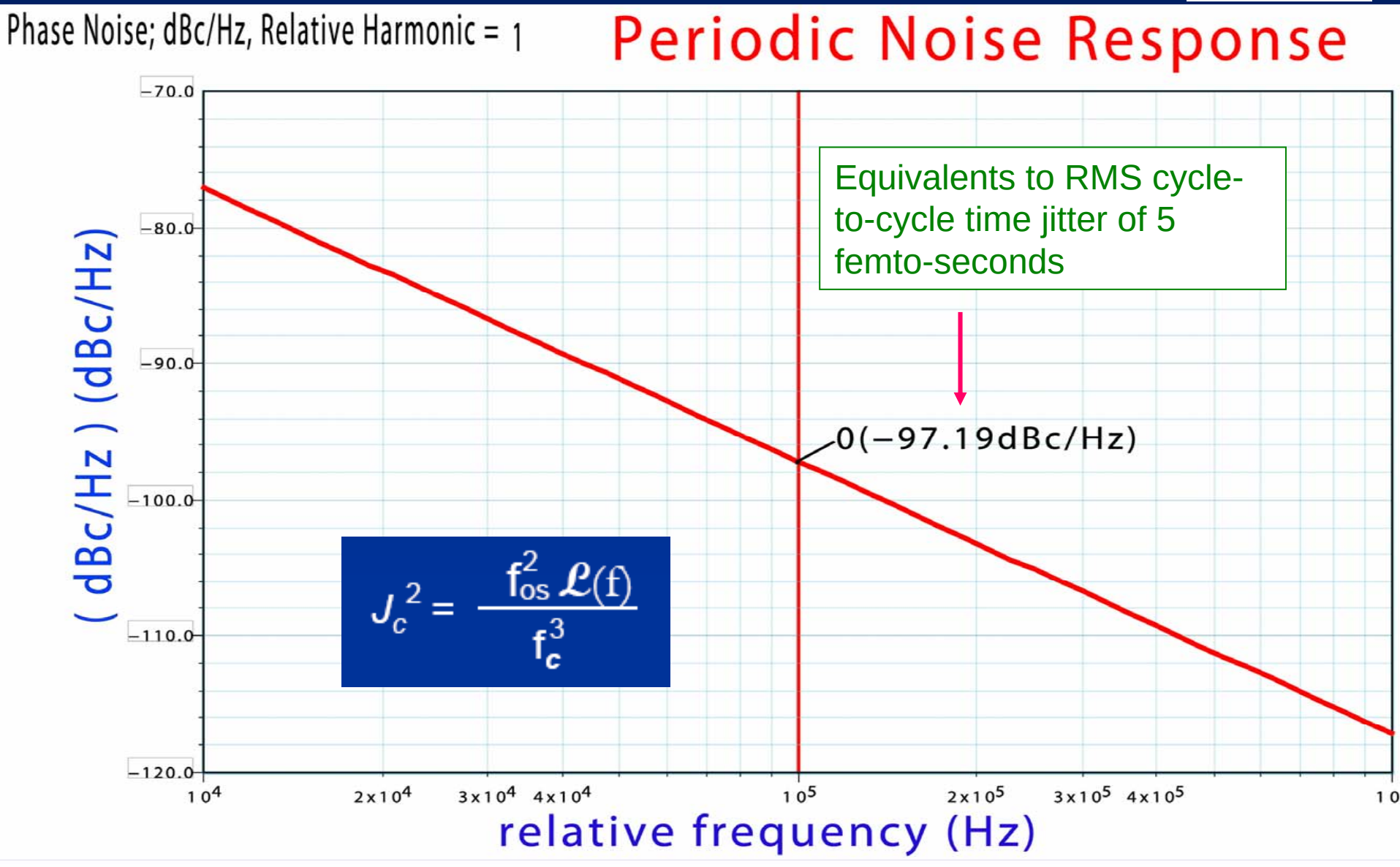
Modify schematic design

Re-layout

Re-simulation

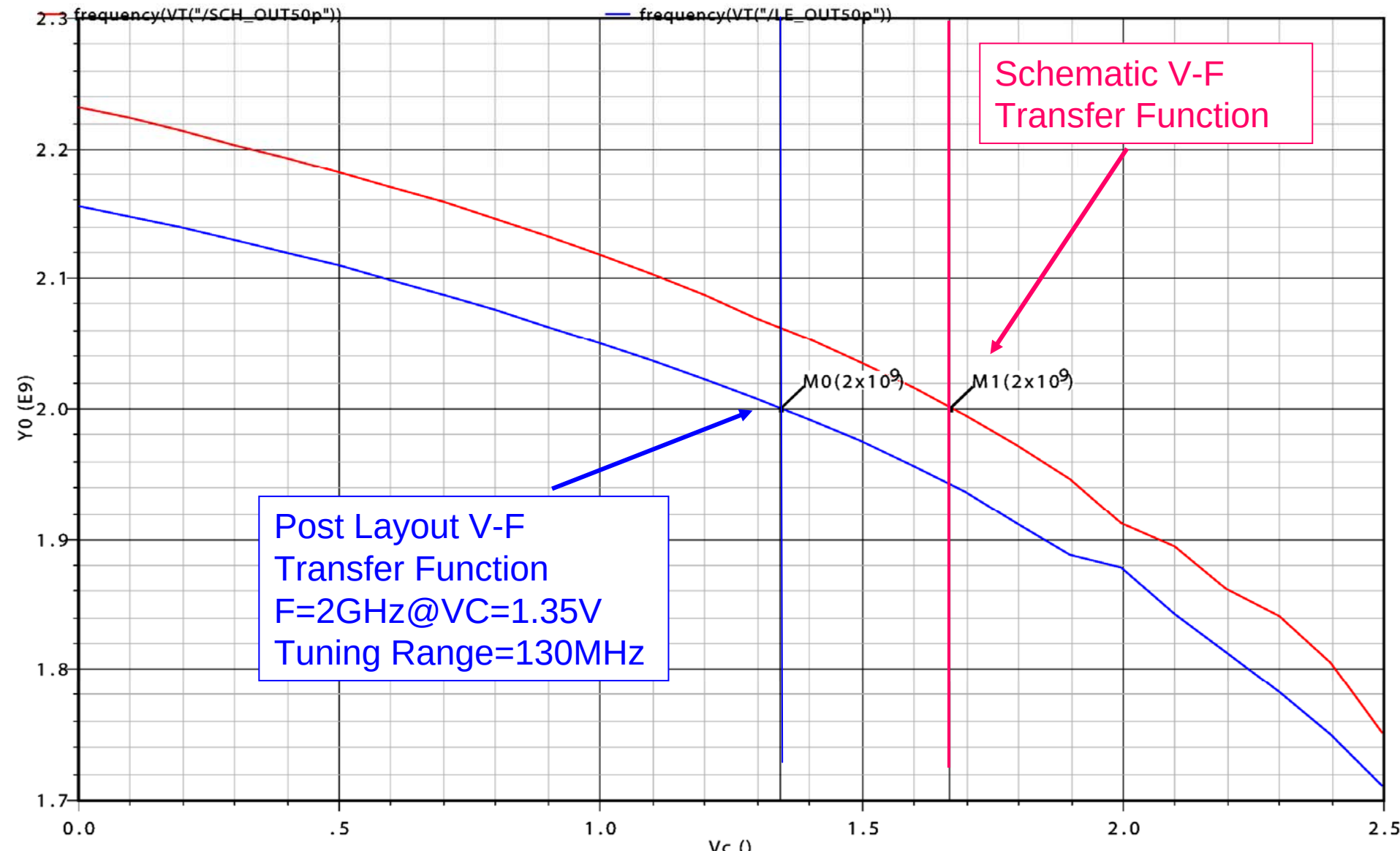
VCO Post Layout Simulation Result (Final)

Output Phase Noise Spectra Plot



VCO Simulation Result (Final)

V-F Transfer Function Plot



Conclusion

(1) IBM 0.13μm SiGe BiCMOS8HP has been evaluated; it is a user-friendly design kit.

(2) Circuit performance meets our requirements (very) well.

(3) MOSIS has resumed 8HP Multi-Project Wafer runs – schedule has been changing(!). We are in the process of understanding how to proceed toward a full chip design starting with our first little VCO chip.

(4) Challenging Issues for the entire readout electronics.

Thanks!