DEVELOPMENT OF A READOUT SYSTEM FOR LARGE SCALE TIME OF FLIGHT SYSTEMS WITH PICOSECOND RESOLUTION

Considerations and designs for a system of tdc's with 1psec resolution

CDF IS TAKEN AS AN EXAMPLE (so we can be definite)

TIME BETWEEN BEAM CROSSINGS =396NS

CHARGED PARTICLES PER COLLISION = APPROX 12

NUMBER OF COLLISIONS/ CROSSING =3

OVERALL SIZE OF DETECTOR ---A CYLINDER 1.5 METER RADIUS AND 3 METER LONG

SIZE OF PROPOSED DETECTOR TILE = 5 CM SQUARE

PROPOSED PIXELS/TILE =4

We require one set of input / output bus lines per 5cm of circumference which results in 189 lines for a 1.5 meter radius cylinder. The cylinder is 3 meters long which means we will have 60 modules per line. Each module covers 5cm square. The total number of 4-cell modules is then 11,340. There will be about 1 event every five collisions in each line of modules assuming 40 charge particles collision

Data generated for each cell per event is about 5 bytes .

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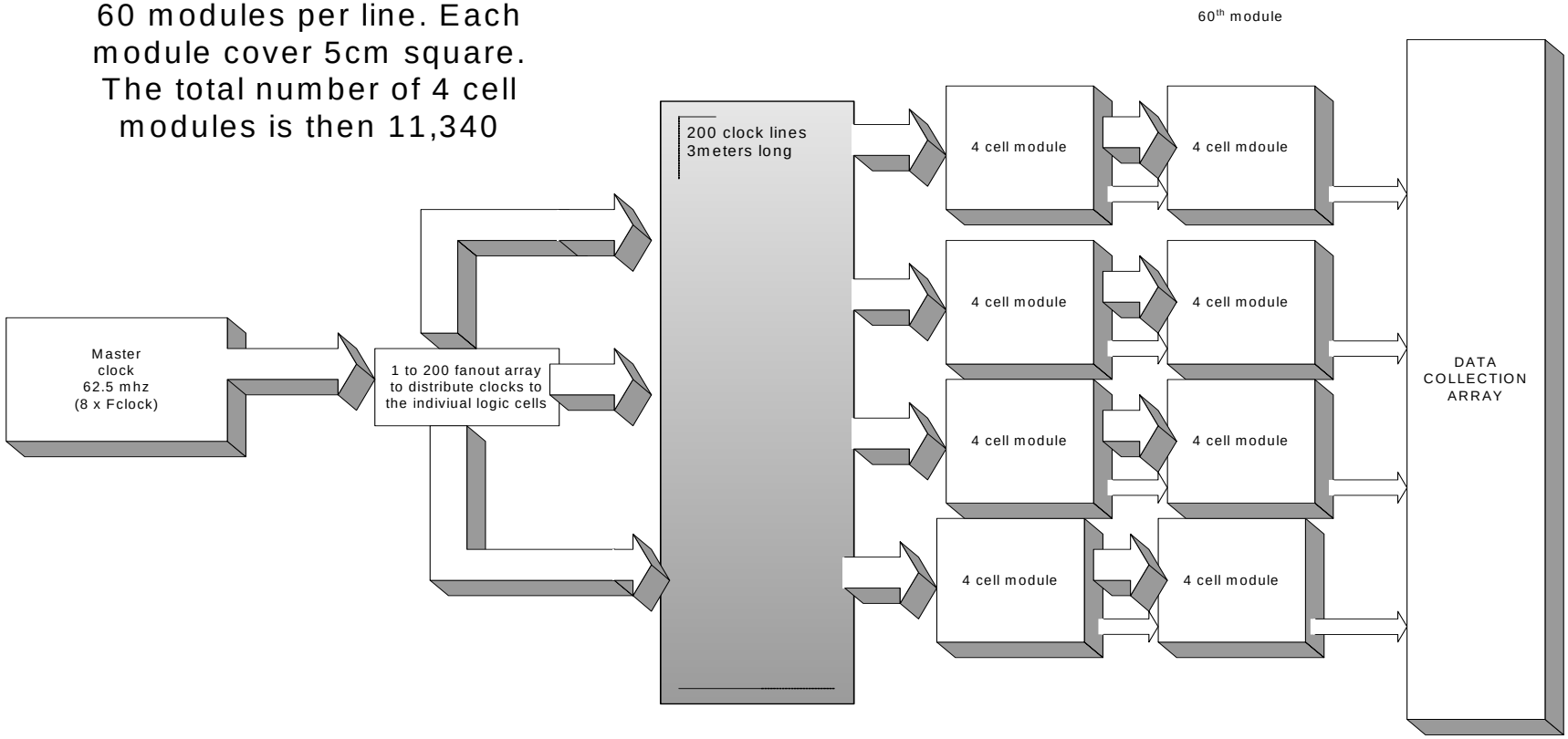
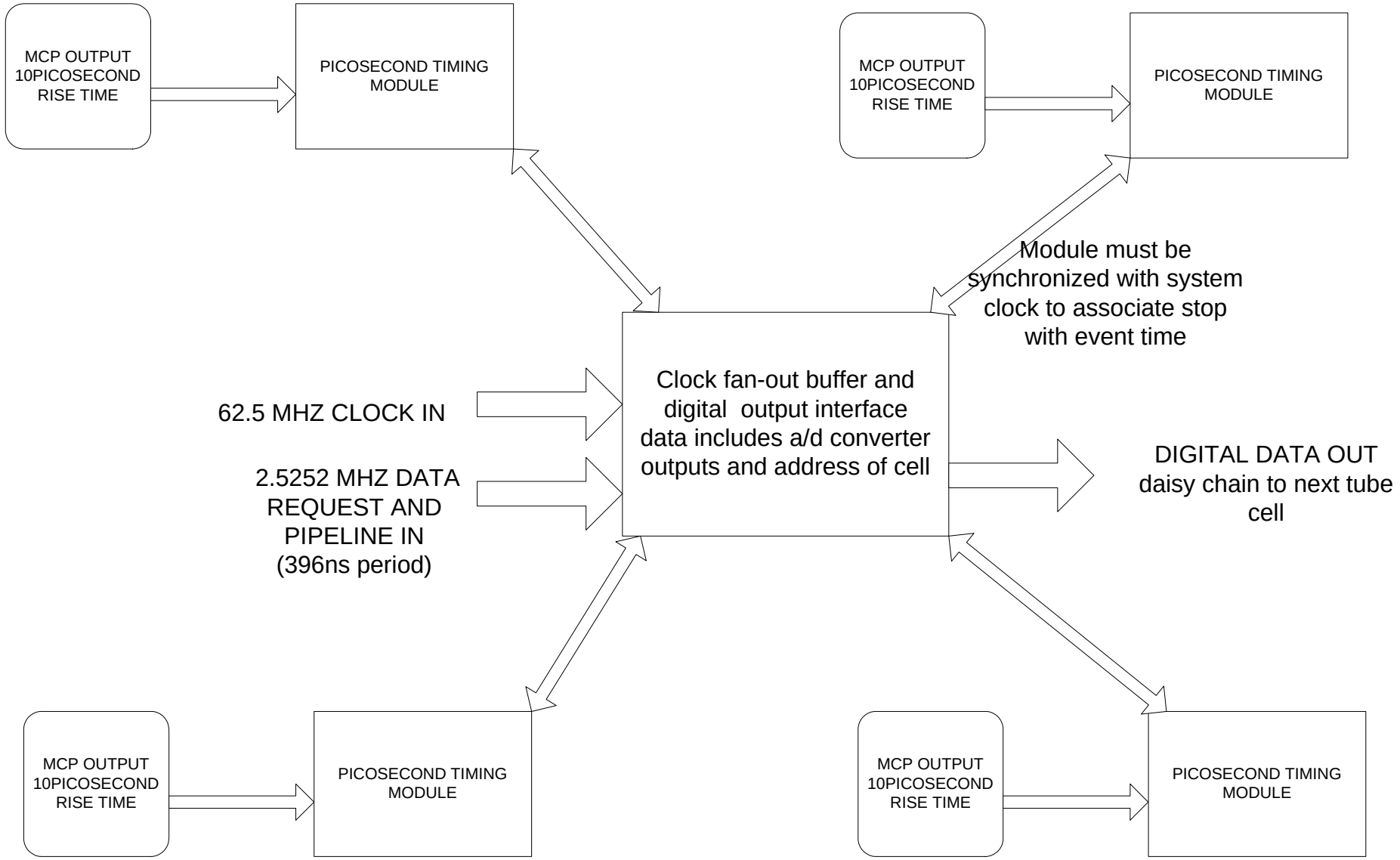
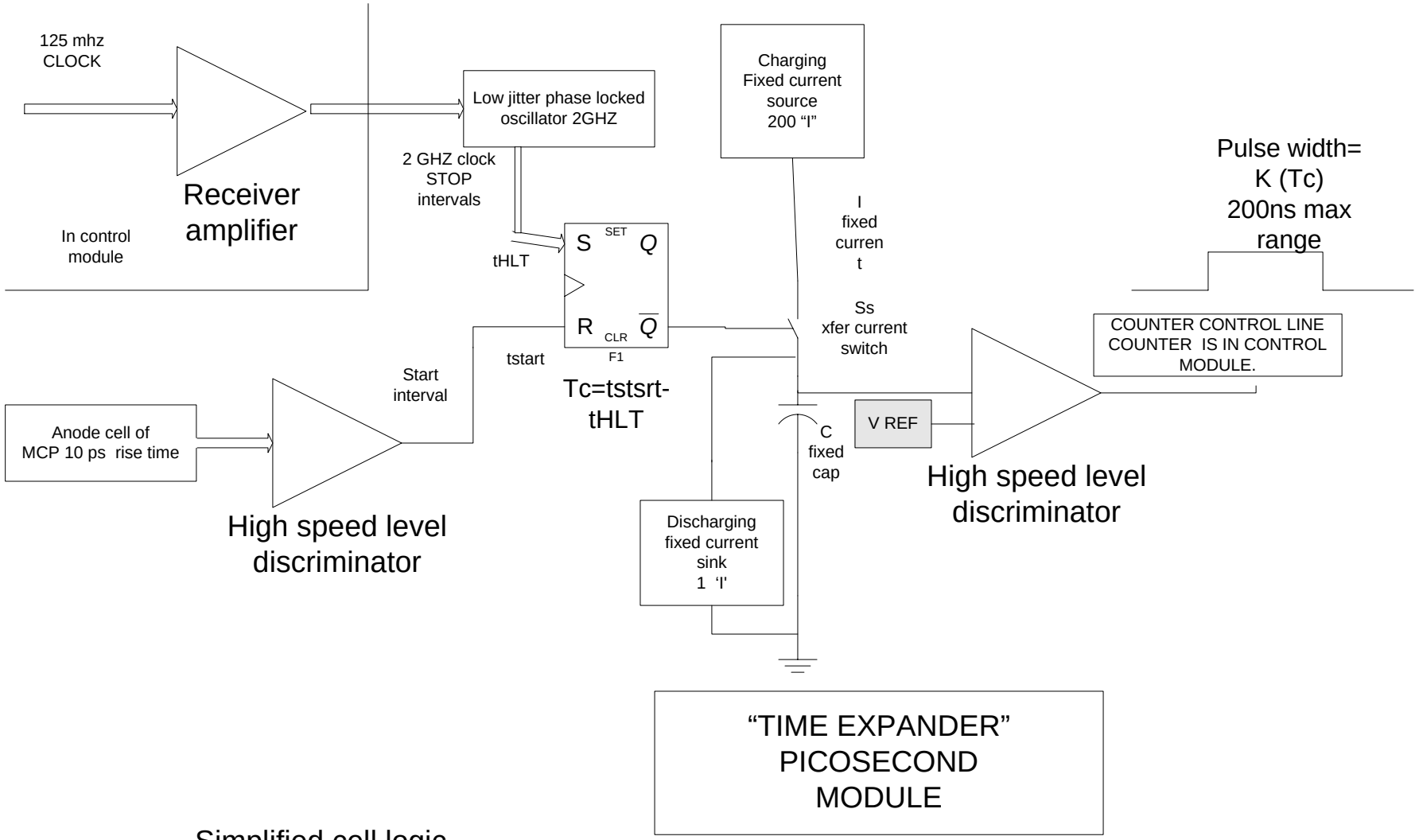


PICO-SECOND TOP BLOCK



4 CELL PICO-SECOND TIMING MODULE



Simplified cell logic
1 0f 4 cells served by
control module

TIME EXPANDER OR DUAL SLOPE PICOSECOND MODULE --- 1 OF 4 PER MCPT

THIS SIMPLE BLOCK DIAGRAM SHOWS A DISCRIMINATOR TO SET A "PULSE GENERATE" STATE FLIP FLOP ON THE LEADING EDGE OF THE TUBE OUTPUT

A CURRENT EQUAL TO 200i CHARGES THE CAPACITOR "C" UNTIL THE STATE FLIP FLOP IS CLEARED AT WHICH TIME THE CAPACITOR IS DISCHARGED AT I EQUAL TO "i" (200 :1)

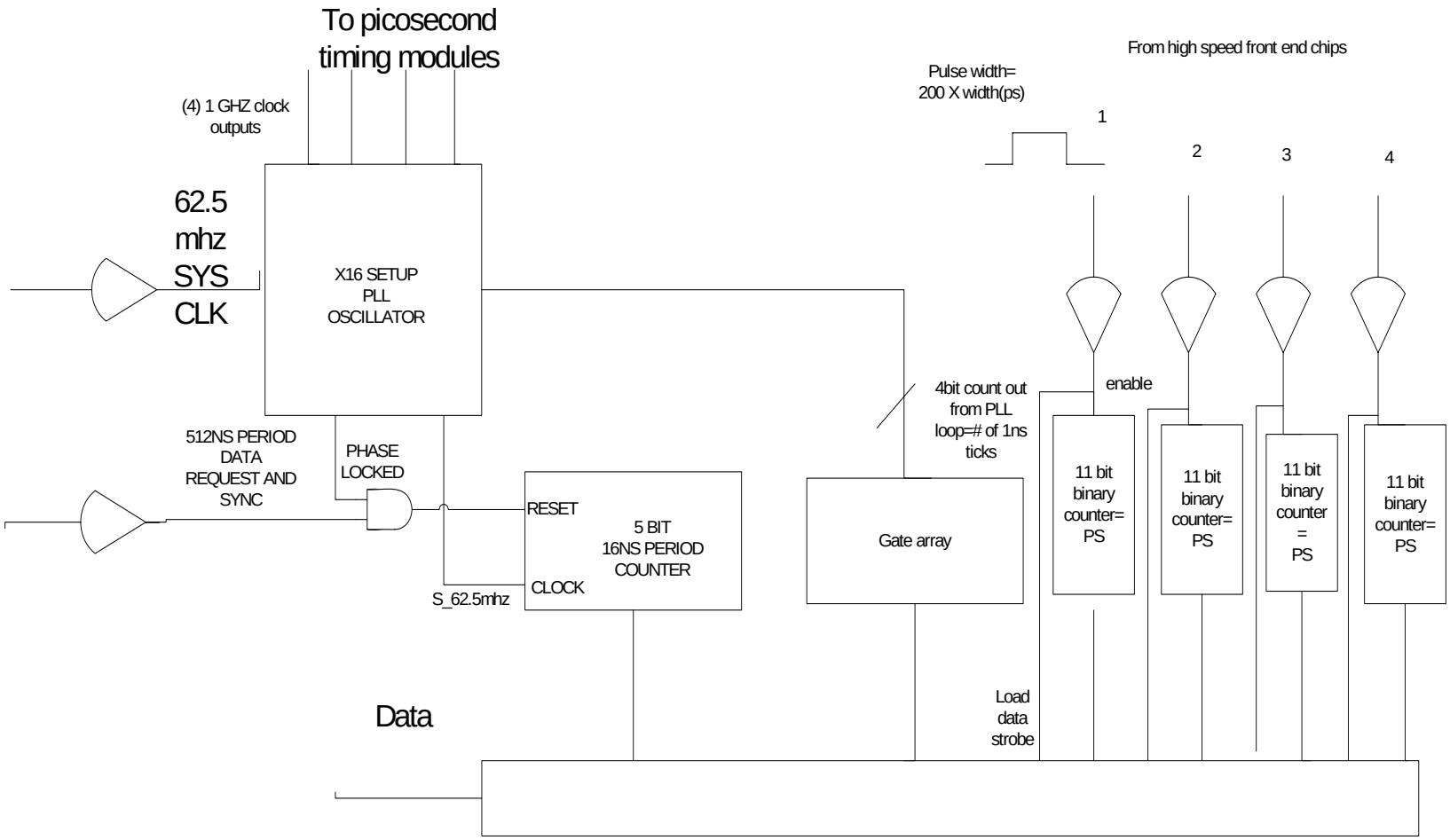
THE DISCHARGE TIME WILL BE 200 TIMES LONGER THAN THE CHARGE.

AN OUTPUT DISCRIMINATOR MEASURES THE PERIOD WHILE THE CAPACITOR IS CHARGED,

THE OUTPUT IS SENT TO THE CONTROL MODULE TO ENABLE A 10GHZ WIDTH-COUNTER AND ALSO SIGNAL THAT AN EVENT HAS HAPPENED.

THE DIFFICULT TASKS THAT MUST BE PERFORMED ARE:

- **THE OSCILLATOR MUST HAE SUB-PICOSECOND JITTER,**
- **THE CHARGE AND DISCHARGE CURRENT MUST BE A STABLE RATIO**
- **200 TO 1 IS LARGE**
- **DISCRIMINATORS MUST HAVE SUB-PICOSECOND STABILITY.**



4 memory blocks 1/per front end–stores16ns,ns, and ps data

CONTROL BLOCK PULSE WIDTH TO COUNT

DESCRIPTION OF CONTROL BLOCK CASE –DIGITAL COUNTER TO MEASURE PICOSECOND INTERVAL

INPUT PHASE LOCK LOOP OSCILLATOR-- SYNCHRONIZE WITH SYSTEM CLOCK

GENERATE 1 GHZ CLOCK FOR PICOSECOND CHIPS

GENERATE 5 GHZ CLOCK FOR PICOSECOND COUNTER CLOCK

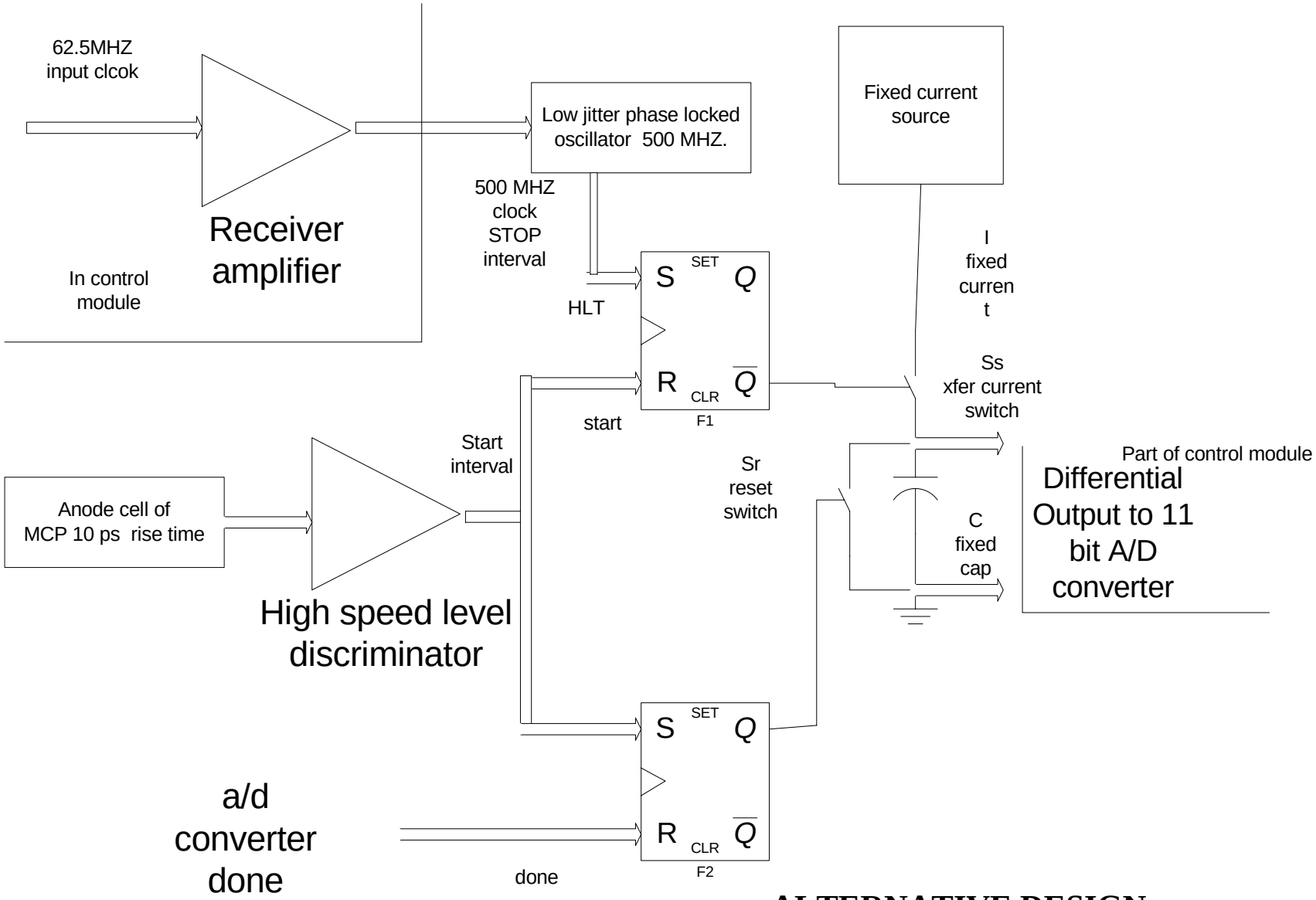
FAST COUNT CLOCKS REDUCE THE TIME STRETCH IN THE PICOSECOND MODULES

THE 512NS SYNC CLOCK IS TIED TO THE COLLISION EVENT MOMENT AND IS USED AS AN EVENT TIME MARKER

A 5 BIT COUNTER TO MEASURE 62.5MHZ (16NS) COUNTS AFTER THE SYNC MOMENT

THE PHASE LOCK LOOP HAS AN INTERNAL COUNTER TO REDUCE THE OUTPUT OF 1GHZ TO 62.5MHZ IN THE CONTROL LOOP. THIS COUNT IS RECORDED TO MEASURE WHICH GHZ TICK (1NS) OCCURRED AT THE EVENT TIME

THE WORD WHICH INCLUDES THE 16NS COUNT,THE NS COUNT AND THE STRETCHED-TIME COUNT GIVES THE TIME OF THE EVENT RELATIVE TO THE SUBJECT EVENT CLOCK PULSE.



Simplified cell logic
1 0f 4 cells served by
control module

ALTERNATIVE DESIGN:

PICOSECOND TIMING MODULE

TIME TO VOLTAGE CONVERTER

DESCRIPTION OF PICOSECOND TO VOLTAGE CONVERTER

CONTAINS THE SAME PRECISION LOCKED OSCILLATOR

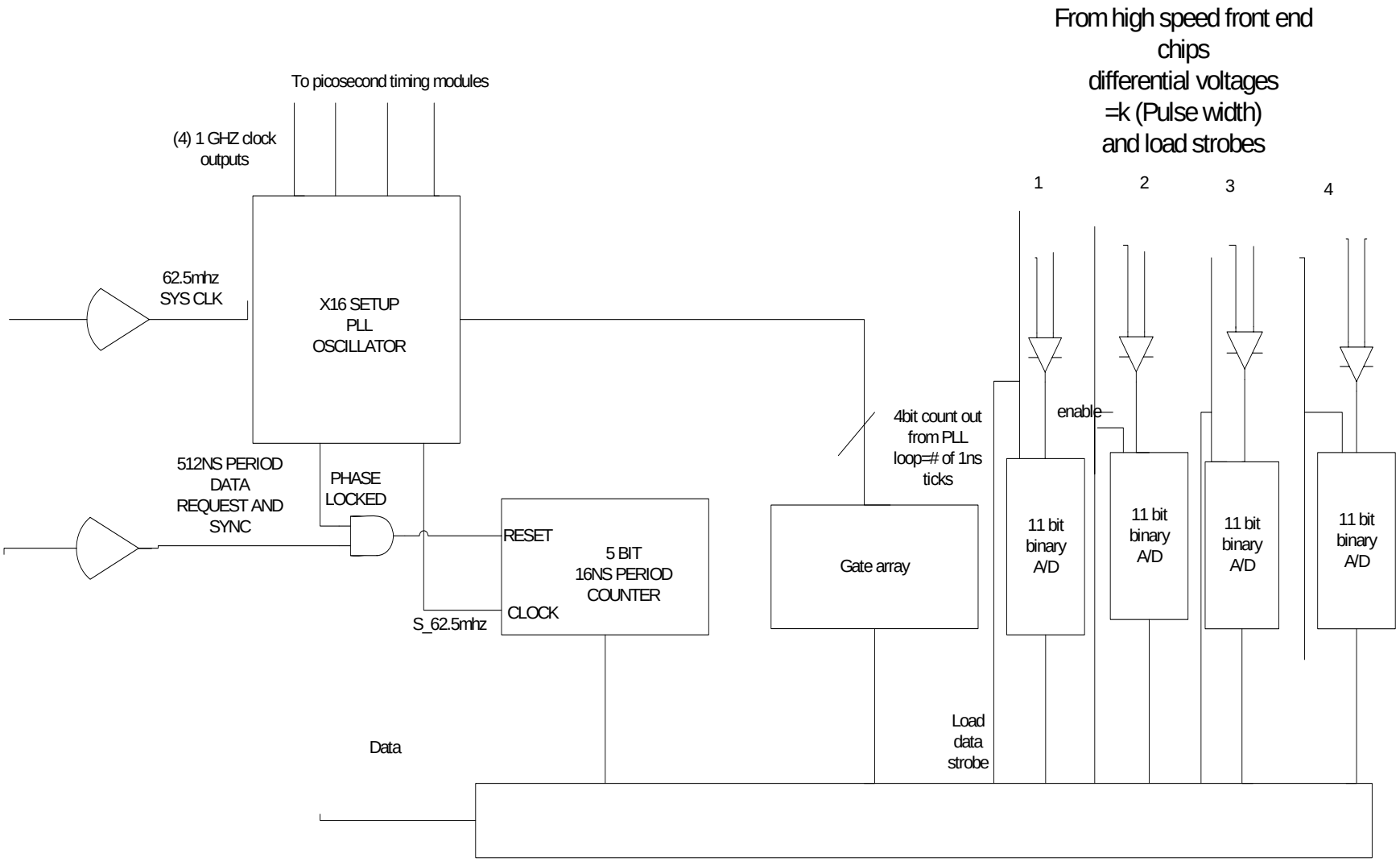
THE EVENT PULSE IS DICRIMINATED AND LATCHES A FLIPFLOP TO START A PULSE.

THE PULSE TURNS ON A CURRENT SOURCE “I” TO CHARGE A CAPACITOR “C”.

THE LOCAL CLOCK GENERATES THE END OF THE PULSE AND THE CURRENT IS INTERUPTED LEAVING A VOLTAGE ON THE CAPACITOR

THE CONTROL MODULE IS SIGNALED TO PERFORM A VOLTAGE CONVERSION (A/D)

A RETURN SIGNAL RESETS THE CAPACITOR TO ITS BASELINE.



4 memory blocks 1/per front end–stores16ns,ns, and ps data

CONTROL MODULE WITH A/D CONVERTERS

DESCRIPTION OF CONTROL BLOCK PICOSECOND TO VOLTAGE CONVERTER

THIS MOULE IS ALMOST IDENTICAL TO THE PULSE WIDTH VARIATION EXCEPT (4) A/D CONVERTERS REPLACE THE COUNTERS

DRAWBACKS TO THIS SOLUTION ARE THAT AN ANALOG SIGNAL MUST BE PASSED BETWEEN THE ENCODER MODULE AND THE CONTROL

THE CONTROL MODULE MUST SIGNAL TO THE FRONT END TO RESET.– THIS LEADS TO MANY MORE CONNECTIONS.

NOTE ON SYNCHRONIZATION OF CHERENKOV PULSE AND LOCAL PRECISION CLOCK

THE EVENT IS ASYNCHRONOUS RELATIVE TO THE LOCAL CLOCK

THERE MUST BE A METHOD TO HANDLE EVENTS THAT HAPPEN CLOSE TO THE CLOCK MOMENT TO ALLOW RECOVERY TIME OF THE MEASURING CIRCUITS.

THE PROPOSAL IS TO ALLOW THE EVENT PULSE TO SET A FLIP FLOP IMMEDIATELY STARTING THE MEASURED INTERVAL.

THIS FLIP FLOP VALUE WILL BE SHIFTED INTO A SECOND FLIP FLOP BY THE CLOCK. THIS FLIP FLOP WILL ALLOW THE CLEARING OF THE FIRST FLIP FLOP ON THE NEXT CLOCK ENDING THE MEASURED INTERVAL

THIS MEANS THE MEASURED INTERVAL WILL BE AS MUCH AS 2 CLOCK INTERVALS, BUT MORE THAN 1.

WE ARE PROPOSING A 1 GHZ CLOCK.

THE MAXIMUM INTERVAL WILL BE 2NS.

WHY USE A SIGE PROCESS?

PUBLISHED PAPERS FROM AN IBM DESIGN GROUP ON USING EARLIER VERSIONS OF THIS PROCESS (5HP) REPORTING PLL OSCILLATORS WITH SUB PICO SECOND JITTER (IBM J RES&DEV VOL 47 NO2/3 MARCH/MAY 2003 SiGe BiCMOS INTEGRATED CICUITS FOR HIGH-SPEED SERIAL COMMUNICATIN LINKS)

- HIGH SPEED
- LOW NOISE

OUR TOOLS, PLANS AND PROBLEMS

TOOLS INCLUDE CADENCE AND MENTOR GRAPHICS DESIGN TOOLS, IBM DESIGN KIT FOR SiGe PROCESS.

WHAT WE MUST DO. WE NEED 2 DIFFERENT CHIPS

DESIGN CHIPS

SIMULATE DESIGN

DESIGN BOARD

ASSEMBLE A SUITABLE TEST FACILITY: EG SCOPES ETC

DESIGN DATA ACQUISTION FOR TESTING

BUY CHIP SAMPLE LOT