April 3, 2011

**FTK Plan up to TDR**

WI: winter SP: spring SU: summer AU: autumn

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| --- | --- | --- | --- | --- | --- |
|  | WORK PACKAGE | TASK | START | COMPLETE | **WHO** |
| 1 | FTK Studies |  |  |  |  |
| 1.1 |  | Complete variable resolution pattern architecture |  | SP 2011 | Guido |
| 1.2 | (hp: hit data/MC) | Compare data and simulation |  | SP 2011 | Jordan, Antonio |
| 1.3 | (high priority) | Robustness to dead channels & modules |  | SP 2011 | Jian |
| 1.4 |  | Use of wild card to improve robustness |  | SU 2011 |  |
| 1.5 | (high priority) | Efficiency and data flow issues |  | SP 2011 | Joe |
| 1.6 | (high priority) | Optimize forward regions |  | SP 2011 | Yangyang |
| 1.7 | (high priority) | Choose the 8 layers (considering μ, π, e) |  | SP 2011 | Bjoern, Guido |
| 1.8 |  | Understand the use of IBL |  | SP 2011 | Constantinos |
| 1.9 | (high priority) | After 1.5-1.7: efficiency, fakes, robustness, b, τ, μ ID |  | SU 2011 |  |
| 1.10 |  | Optimize pixel clustering, especially IBL |  | SP 2011 |  |
| 1.11 |  | Optimize criteria for HW selecting among duplicate tracks |  | WI 2012 |  |
| 1.12 |  | Performance if 2 misses are allowed |  | WI 2012 |  |
| 1.13 | (high priority) | Quality and number of tracks out of stage 1 |  | SP 2011 |  |
|  |  |  |  |  |  |
| 2 | Trigger Studies |  |  |  |  |
| 2.1 |  | Improved b-tagging algorithm |  | SP 2011 | Antonio |
| 2.2 |  | L1,L2 e trigger |  | WI 2012 | ANL/NIU |
| 2.3 |  | Check b, τ, μ, e results on data |  | SU 2011 |  |
| 2.4 |  | Incorporate FTKSim into ATHENA |  | SU 2011 | FTK & HLT |
| 2.5 |  | How to use FTK tracks in HLT selection |  | SU 2012 | FTK & HLT |
| 2.6 |  | Handling FTK errors in HLT |  | SU 2012 | FTK & HLT |
|  |  |  |  |  |  |
| 3 | Hardware |  |  |  |  |
| 3.1 |  | Design specs: ext./int. comm., FIFOs, SpyBuffers, errors, |  | SP 2011 | All |
| 3.2 |  | HOLA |  |  |  |
| 3.2.1 |  | firmware |  | WI 2011 | Anton |
| 3.2.2 |  | 1st prototype |  | WI 2011 | Tang |
| 3.2.3 |  | testing |  | SP 2011 | Anton |
| 3.2.4 |  | production |  | AU 2011 | Tang |
| 3.3 |  | AM chip |  |  |  |
| 3.3.1 |  | design | 11-2010 | SP 2011 | Stabile/Beretta/  Hoff/Solveit/Liberali |
| 3.3.2 |  | simulation | 12-2010 | SU 2011 | Crescioli/Sacco/Bossini |
| 3.3.3 |  | 1st submission |  | AU 2011 |  |
| 3.3.4 |  | testing |  | SP 2012 | All |
| 3.4 |  | AM board |  |  |  |
| 3.4.1 |  | schematics | 1-2011 | SP 2011 | Piendibene/Andreani |
| 3.4.2 |  | firmware | 1-2011 | SU 2011 | Piendi./Magal./Andreani |
| 3.4.3 |  | simulation |  | SU 2011 | Piendi./Andreani/Stabile |
| 3.4.4 |  | 1st prototype – placing & routing | SU 2011 | AU 2011 | CERN e-shop |
| 3.4.5 |  | test | WI 2011 | SP 2012 | Piendi./Magal./Andrea. |
| 3.5 |  | LAMB |  |  |  |
| 3.5.1 |  | schematics | 1-2011 | SP 2011 | Lanza/Giannetti |
| 3.5.2 |  | firmware | 1-2011 | SU 2011 | Piendibene/Lanza |
| 3.5.3 |  | Simulation of critical lines | 2-2011 | SU 2011 | Piendibene/Lanza/Stabile |
| 3.5.4 |  | 1st prototype – placing & routing | SU 2011 | AU 2011 | Pavia e-shop |
| 3.5.5 |  | test | WI 2012 | SP 2012 | Lanza/ Piendibene |
| 3.6 |  | Data Formatter mezzanines |  |  |  |
| 3.6.1 |  | schematics | 2010 | SP 2011 | Gatta/Pellegrini |
| 3.6.2 |  | firmware | 2009 | SP 2011 | Beretta-Annovi |
| 3.6.3 |  | simulation | 2009 | SP 2011 | Beretta-Annovi |
| 3.6.4 |  | 1st prototype– placing & routing | AU 2010 | SP 2011 | Gatta/Pellegrini |
| 3.6.5 |  | test | SP 2011 | SU 2011 | Beretta-Annovi |
| 3.7 |  | Data Formatter board |  |  |  |
| 3.7.1 |  | backplane connections & crate format |  | SP 2011 |  |
| 3.7.2 |  | specify “service” tasks of the DF |  | SP 2011 |  |
| 3.7.3 |  | schematics |  | AU 2011 |  |
| 3.7.4 |  | I/O firmware |  | WI 2012 | Holing |
| 3.7.5 |  | “service” firmware |  | WI 2012 |  |
| 3.7.6 |  | simulation |  | SP 2012 |  |
| 3.7.7 |  | 1st prototype |  | SU 2012 |  |
| 3.7.8 |  | test |  | AU 2012 |  |
| 3.8 |  | AM AUX board (firmware: student,Mel,Florencia,Mircea) |  |  |  |
| 3.8.1 |  | board to test VME and P3 connections to AM board | 04-2011 | SP 2011 | Mircea |
| 3.8.2 |  | schematics | AU 2010 | AU 2011 | Mircea |
| 3.8.3 |  | DO-WR firmware | 03-2011 | SU 2011 | Yangyang |
| 3.8.4 |  | DO-RD firmware | 09-2011 | WI 2012 | Yangyang |
| 3.8.5 |  | TF firmware | 03-2011 | WI 2012 | Jordan |
| 3.8.6 |  | I/O firmware | 03-2011 | WI 2012 | Mircea |
| 3.8.7 |  | HW firmware (after Illinois completes its work) | 03-2012 | SP 2012 |  |
| 3.8.8 |  | simulation | SU 2011 | SP 2012 | Mircea & students |
| 3.8.9 |  | 1st prototype | SP 2012 | SU 2012 | Mircea |
| 3.8.10 |  | test | SU 2012 | AU 2012 | Students & Mircea |
| 3.9 |  | 2nd-stage board |  |  |  |
| 3.9.1 |  | schematics | 03-2011 | AU 2011 | Mark & Mike |
| 3.9.2 |  | I/O firmware | 08-2011 | WI 2012 | Viviana/new postdoc |
| 3.9.3 |  | extrapolation firmware | 08-2011 | WI 2012 | Viviana/new postdoc |
| 3.9.4 |  | HW firmware | 09-2011 | WI 2012 | Markus |
| 3.9.5 |  | TF firmware (after Chicago finishes) | 03-2012 | SP 2012 | Markus |
| 3.9.6 |  | simulation | SU 2011 | SP 2012 | New student & Mike |
| 3.9.7 |  | 1st prototype | SP 2012 | SU 2012 | Mike |
| 3.9.8 |  | test | SU 2012 | AU 2012 | Mike & students |
| 3.10 |  | Connection to level-2 |  |  |  |
| 3.10.1 |  | modeling/evaluation of FTK-ROS dataflow scenarios | 03-2011 | 09-2011 | Andrea Negri |
| 3.10.2 |  | specification & tests | 03-2011 | 02-2012 | John/Jinlong |
| 3.10.3 |  | schematics | 02-2012 | 06-2012 | John/Gary |
| 3.10.4 |  | firmware | 06-2012 | 09-2012 | John/Andrew |
| 3.10.5 |  | simulation | 06-2012 | 09-2012 | John/Andrew |
| 3.10.6 |  | 1st prototype | 09-2012 | 03-2013 | John/Todd/Dennis |
| 3.10.7 |  | test | 03-2013 | SU 2013 | Jinlong & student |
|  |  |  |  |  |  |
| 4 | vertSlice/integration |  |  |  |  |
| 4.1 |  | Validate SLIM AM board with EDRO | 10-2010 | SP 2011 | Piendi./Mag./Villa/Cresc. |
| 4.2 |  | Test DF mezzanine on EDRO | SP 2011 | SU 2011 | + Annovi- Beretta |
| 4.3 |  | Build SLIM AM boards for cooling tests | AU 2011 | AU 2011 | Piendi-Giannetti |
| 4.4 |  | Cooling tests | SP 2012 | SP 2012 | Piendi-Giannetti |
| 4.5 |  | Move vertical slice to CERN |  | AU 2011 | Piendi./Mag./Villa/Cresc. |
| 4.6 |  | Implement FTK-ROS connection | 03-2011 | WI 2012 | Mauro/Filippo/Andrea/ Jinlong |
| 4.7 |  | Data Organizer firmware in EDRO | SP 2011 | SP 2012 | Villa/Giorgi |
| 4.8 |  | Insert GigaFitter or fit in CPUs | WI 2012 | SP 2012 | Crescioli |
| 4.9 |  | Install vertical slice in ATLAS | SP 2012 | SU 2012 | ALL |
| 4.10 |  | Software development for the vertical slice | 10-2011 | SU 2012 | Crescioli, Cervigni & students |
|  |  |  |  |  |  |
| 5 | TDR |  |  | SU 2013 |  |
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