Towards a Level-One Tracker Trigger for SLHC-CMS

Zhenyu Ye/Fermilab
Outline

• Introduction
• Level-One Tracker Trigger for SLHC-CMS
  – VICTR: Vertically Integrated CMS Tracker ASIC
  – Oxide Bonding and Active Edge Silicon Sensor
• Summary and Outlook
The CMS Detector

3.8 T solenoida B field; Lead-Tungstate Crystal ECAL; Brass/Scintillator HCAL. Gas-detectors for muons embedded in return yoke.

All Silicon Tracker: pixel+strip world largest silicon device, ~200 m², >70 million channels
The CMS Trigger System

- **Level-1 Trigger**: Custom made hardware processor.
- **High Level Trigger**: PC Farm using reconstruction software and event filters similar to the offline analysis.
  - 40 MHz input rate at L1
  - 100 KHz input rate for HLT
  - 100 Hz written at the output
  - 128 Bx = 3.2 µsec L1 latency
  - Event Size 1-2 Mbytes
  - **Impossible to read out all tracking channels at L1**
The CMS L1 Trigger System

- Current L1 trigger decision is based on the calorimeter and muon detector.
- At L1 we trigger on:
  - high $E_T$ $e^+/\gamma$
  - high $P_T$ muons
  - high $E_T$ jets
  - high $E_T$ tau’s
The SLHC

By 2018 the gain of running LHC longer will be limited. A luminosity upgrade is planned thereafter....
The SLHC

- 200-400 interactions/25 ns crossing at the SLHC
At the SLHC, electron, jet, tau and muon triggers will fire in the MHz region (with the LHC thresholds). Keeping the same thresholds as at LHC may be desirable if one wants to study possible LHC signals with more statistics.

Even if one wished to raise threshold it would not help as shown in the muon trigger case.
L1 Tracker Trigger for SLHC-CMS

• CMS at the SLHC
  – L1 trigger rate based on calorimeter and muon detector will saturate
  – Tracking info has to be included for L1 trigger decision

• Need a track trigger to be able to
  – Identify and provide a Z vertex resolution of ~1mm for tracks with $p_T$ above ~2.5 GeV at L1 (e/μ/tau track isolation, particle flow jet)
  – Identify and provide a Z vertex resolution of ~1mm for tracks with $p_T$ above ~15 GeV at L1 (e/μ track match)
  – provide full event readout upon HLT trigger accept

• Track $p_T$ and Z need to be determined “locally”
  – Unacceptable power and bandwidth required to transmit all hit information from the tracker to an external trigger processor
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A filter for high $p_T$ track hits based on the impact parameter of the hits on two adjacent layers of silicon detectors.
Don’t need fine Z resolution on both layers:

- long strip: 5-10 mm x 100 μm
- short strip: 1-2 mm x 100 μm
- 1 long strip vs 5 short strips
L1 Track Trigger Design

- Pixelated silicon sensor to allow both $\phi$ and $Z$ position measurement for hits on the detector.
- Two layers of silicon sensors separated by $\sim 1\,\text{mm}$ for local high $p_T$ track hits filtering and track stub formation.
- Multiple double-layers for track reconstruction.
L1 Track Trigger Design

One single readout chip connects to both the top and bottom sensors

- Analog information from the top sensor is passed to the ROIC through a PCB interposer
- reconstruct hits locally for each sensor
- correlate hits from the top and bottom sensors to form track stubs
- provide the reconstructed track stubs for L1 track reconstruction
- provide the full event info upon L2 accept
How to Build – 3D Integration

- A **vertically (3D) integrated circuit** comprised of 2 or more layers of CMOS devices which have been thinned, bonded, and vertically interconnected to form a “monolithic” circuit. These layers can be devices made in different technologies.

- A major direction in semiconductor industry:
  - Reduces trace length; Reduces R, L, C;
  - Improves speed; Reduces interconnect power, crosstalk;
  - Reduces chip size; Processing for each layer can be optimized.
How to Build – 3D Integration

- Bonding between layers
  - Cu-Cu
  - Si Oxide
  - Cu-Tin
  - Polymer/adhesive
- Wafer thinning
  - grinding, lapping, etching, CMP
- Through silicon via formation
- High precision alignment

Cu-Cu bonded two-tier IC (Tezzaron)
How to Build – 3D Integration

4 The top sensor is bump-bonded to the PCB Interposer making a complete device.

3 Bumps are placed on the top sensors

2 The PCB Interposer is bump-bonded to the 3D ROIC

1 The 3D ROIC is oxide-bonded to the bottom sensor and then thinned.
L1 Track Trigger Design

One single readout chip for two silicon sensors, one sensor connected from the top through the interposer and the other from the bottom

- The top sensor has “long” strips (5mm*0.1mm)
- The bottom sensor has “short” strips (1mm*0.1mm)
L1 Track Trigger Design

- Module design assumes a 5x6 array of chips.
- There is a placement yield for each chip, unless this yield is very close to 100% this design will be too costly.
- Use known good sensor/ROIC and high yield bump bonds to connect to PCB.
- Smaller modules are problematic because saw cut edges on normal silicon are sources of leakage current. Usually stay 3x depth away to limit leakage current - creates dead areas.
- Use edgeless silicon sensor.
## Technical Feasibility

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<td>An interposer technology with low mass</td>
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<td>R&amp;D on using active edge sensors combined with 3D chips</td>
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VICTR chip: two tiers vertically integrated with Cu-Cu bonding

- Each tier has its own set of shifter registers, digital-to-analog converters for frontend bias, and signal amplification-shaping-discriminating.
- Transfer discriminator outputs from the top long strip tier to the bottom short strip tier through TSVs and Cu-Cu bonding interconnects.
- Readout architecture exists in the bottom short strip tier only.
The VICTR Chip

- Two tiers vertically integrated with Cu-Cu bonding – “3D chip”.
- Each tier is able to work on its own – “2D chip”.

Short Strip Tier before thinning

Power

I/O

700 micron
VICTR Chip Design

- Frontend A-S-D design from LBNL (A.Mekkaoui and J.Fleury)
- Control DACs design from CPPM (J.Clemens, P.Pangaud, S.Godiot)
- Readout architecture by Fermilab ASIC design group (J.Hoff et al.)

Gain = 40.0 mV/fC @ Cin=1.0 pF; tpeak = 40 ns
  = 36.8 mV/fC @ Cin=2.0 pF; tpeak = 59 ns
  = 43.0 mV/fC @ Cin=0.1 pF; tpeak = 21 ns
VICTR Chip Fabrication

• Fabricated in the first HEP 3D multiproject run in Tezzaron 0.13 micron CMOS process.
• 2D chips tested in the summer.
• 3D chips received in September 2011.
Tests for 2D Chips

- chip register download
- frontend bias control
- frontend ASD response
- backend readout

![Threshold 2D Map](image1)

![Noise 2D Map](image2)

![Threshold Scan For Strip[0,0]](image3)

![Threshold Distribution](image4)

![Noise Distribution](image5)

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Kill Map Downloaded to Chip (to disable some strips)

Hit Map from Charge Injection (consistent with kill map)
3D Chip Testing Results

- Tested 3D chips in which either the short or the long strip tier was thinned.
- Shift register download ok for both long and short strip tiers for all 3D chips.
- Frontend bias control ok for both long and short strip tiers for all 3D chips.
- See discriminator outputs from the short strip tier in response to charge injection, but not from the long strip tier in response to charge injection.
- Similar A-S-D responses for the short strip tier among 3D chips, and to 2D chips.
Interconnection Between Tiers

Connection between two tiers

Cu-Cu bonding array

Connection for power or I/O pads

Connection for power or I/O pads
Interconnection Between Tiers

Connection between two tiers

Cu-Cu bonding array

Connection for discriminator output
3D Chip - Misalignment

Top Pads deposited after thinning

Through silicon vias

6 micron

Top (long strip) electronics

Cu bond interface

Bottom (short strip) electronics

Missing contacts

700 micron

6 micron
Top Pads deposited after thinning through silicon vias.

Bobom (short strip) electronics and Cu bond interface

M6 top and M6 bottom (long strip) electronics

Missing contacts 6 micron

700 micron

• misalignment of bonding interface

• SEM picture courtesy of P. Siddons BNL

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3D Chip Testing

• First VICTR 3D Chip passed the smoke test
  – Download shift register between top and bottom layers works
  – Power controls work
  – Strip kill test working on short strip tier

This tests the backside thinning, exposure of the through-silicon-via, and Cu-Cu bonding, which is all needed for the Track Trigger.

• The first pair of bonded wafer appears to have alignment problems

• 12 more wafers (6 pairs) available for processing

Issues with this bond

This process is OK
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How to Build – 3D Integration

1 The 3D ROIC is oxide-bonded to the bottom sensor and then thinned.

2 The PCB Interposer is bump-bonded to the 3D ROIC

3 Bumps are placed on the top sensors

4 The top sensor is bump-bonded to the PCB Interposer making a complete device.
Oxide Bonding

- 3D IC vendors with commercially available bonding process
  - Tezzaron – Cu-Cu thermo-compression for bonding
  - Zycube – Adhesive and In-Au bump for bonding
  - Ziptronix - Direct Bond Interconnect based on oxide bonding

- Fermilab has worked with Ziptronix to demonstrate the DBI technology for particle physics sensor/ROIC integration.

2/13/2012
**DBI Technology**

- Oxide bonding at room temperature.
- Metal connection by thermo-compression.
- Robust mechanical connection – sensor/IC can be ground and thinned after bonding.
- 3 µm pitch achieved; also Low mass.
- Die to wafer, wafer to wafer.
- ROICs can be placed onto sensor wafers with 10 µm gaps – pave the way towards thinned full coverage detector planes.
- Could be fairly inexpensive (esp. w2w).
L1 Track Trigger Design

- Module design assumes a 5x6 array of chips.
- There is a placement yield for each chip, unless this yield is very close to 100% this design will be too costly.
- Use known good sensor/ROIC and high yield bump bonds to connect to PCB.
- Smaller modules are problematic because saw cut edges on normal silicon are sources of leakage current. Usually stay 3x depth away to limit leakage current - creates dead areas.
- Use edgeless silicon sensor.
Active Edge Silicon Sensor

Trench filled with polysilicon

Sensor Wafer  Implant  Aluminum
Handle Wafer  polysilicon
(a) Conventional structure

- Multiple guard rings
- Strips or pixels
- Conventionally diced edge

(b) Edgeless structure

- Stop Ring (SR)
- DRIE diced edge
- Strips or pixels
- Phosphorus ions
Active Edge Silicon Sensor

- p+ diodes on n- bulk ($\rho=5k\Omega\cdot cm$);
- 22 column x 128 rows
  - 50x600 µm for 1st and 22nd column
  - 50x400 µm for 2nd-21st column
- 50 µm deep n++ trench at the edge:
  - can use it as a high quality detector edge;
  - can use it as an electrode – eliminating edge losses in tiling reticle-sized detectors.
- masks designed at Fermilab;
- fabricated by MIT-Lincoln Lab.

Sensor cross section

- p+ diode implant
- n++ trench connected to bottom implant
- bottom implant
Active Edge Silicon Sensor

Sensor bias scheme:
- p+ diodes (DBI) connected to FPIX input at ground potential;
- n++ trench (DBI) connected to positive potential through FPIX.

The electrical connection from the trench to the ground surface of the backside might be either (a) along the surface and cut edge or (b) by punch-through 50 μm bulk.

(optional) n+ pinning layer surrounding p+ diodes and extended to trench:
- commonly used in optical devices to passivate the detector surface;
- could act as a shield between the detector and ROIC.
DBI Prototypes

- **Active edge pixel sensor:**
  - p+ diodes on n- bulk ($\rho=5k\Omega\cdot cm$);
  - 22 column x 128 rows
  - 50 µm deep n++ trench at the edge
  - masks designed at Fermilab;
  - fabricated by MIT-Lincoln Lab.

- **BTeV FPIX2.1 readout chip:**
  - 22x128 (C*R) pixel cells of 50x400 µm;
  - designed for e- signals (3 bits ADC), can work with small hole signals but Y/N only;
  - can inject test pulse to capacitor (~3.5fF);
  - debugging pads available for analog and digital output of the pixels in the last row.
DBI Prototypes

- 50 MIT_LL sensors DBI bonded to two FPIX wafers by Ziptronix.
- Sensors thinned to 100 µm after bonding, backside not implanted.
- 30 good devices at the end (16 with bond voids indicated by SAM. Normal yield is 80-90% if not dealing with a small number of wafers as us).

A DBI bonded FPIX wafer by Ziptronix

Scanning Acoustic Microscopy
DBI Prototypes

A integrated device after dicing

FPIX2.1
ROIC

sensor (backside)

9.9mm

7.1 mm
Threshold Scan

Conversion from the test pulse size to the number of electrons done assuming 3.5fF injection capacitors.

S-curve for pixel (10,10)

threshold=3894 e-
noise=98 e-
Sensor with Bond Void

c) sensor with bond void

Scanning Acoustic Microscopy
We are able to see the digital outputs of >99% of the channels due to the laser and due to a β source (Sr-90).
Test Beam Test

- Fermilab Meson Test Beam Facility 120 GeV proton beam perpendicular to the telescope and DET.
- Two telescope stations of BTeV pixel sensors, with one bit of digital output (“hit”) from each 50x400µm pixel unit.

- X/Y positions of the reconstructed hits are “semi-discrete”.

[Diagram showing proton beam direction and station layout]
Test Beam Test

Graph 1: Scatter plot of expected x (mm) vs. measured x (mm)

Graph 2: Scatter plot of expected y (cm) vs. measured y (cm)
Test Beam Test

Column $2^{nd}$-$21^{st}$ : $400 \times 50 \, \mu m$
Test Beam Test

Column 1\textsuperscript{st} and 22\textsuperscript{nd} : 600 x 50 µm
Summary and Outlook

• Work towards a proof of concept for a L1 Tracker Trigger for SLHC upgrade with vertical integration techniques.

• A prototype frontend ASIC has been designed and fabricated, and is currently being tested.

• Initial tests suggests that 3D techniques needed for a tracker trigger ASIC are basically working. More studies are underway.

• Some issues discovered with the first prototype chip design and fabrication. Will be considered for the next chip design.
Summary and Outlook

• The DBI technology as a replacement of bump-bonding for particle physics pixel sensor/ROIC integration:
  – Low mass, fine pitch;
  – Sensor/ROIC thinning possible after bonding;
  – Available commercially, fairly inexpensive.

• Tests of DBI bonded devices promising:
  – Active edge pixel sensor mated to FPIX2.1 chip;
  – A very small number of interconnect failures;
  – Sensor input capacitances seem to be small.
  – Radiation damage for DBI bonding done
Plans for 2012-2013

Test 3D Chip
  Integrate with sensor
  Bond to stack
  Test

Module Bump bonding
  Test assembly
  Iterate with interposer II
  Test

Design Data flow chip
  Fabricate
  Test
  Mechanical Design

Active edge sensor design
  Sensor Fabrication
  Tile Production
  Assembly bump bond
  Test

Interposer + dummy sensor
  Fabrication

Demonstration Stack

2/13/2012

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Backup Slides Start Here
CMS Silicon Tracker

World Largest Silicon Device
200 m², >70 million channels
3 layers of pixels, 10 layers of strips
CMS Data Taking

Rapid increase in instantaneous luminosity:
April \( L = 2.0 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1} \)
October \( L = 3.5 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1} \)
The Lv1 Algorithms

Electron/Photon triggers:
- Electron (Hit Tower + Max)
  - 2-tower $\Sigma ET$ + Hit tower $H/E$
  - Hit tower 2x5-crystal strips >90% ET in 5x5 (Fine Grain)
- Isolated Electron (3x3 Tower)
  - Quiet neighbors: all towers pass Fine Grain & $H/E$
  - One group of 5 EM ET < Thr.

Forward Central and Tau Jet Triggers
- Search for $E_\tau$ bumps within 12x12 Trigger Tower (TT) window (1 TT= 0.087x0.087)
- Sort in $E_\tau$ and transmit the 4 highest $E_\tau$ jets + position information to the Global Trigger.
- Tau-Jets are central jets which have tau-Veto off (collimation cut)
The Challenges at SLHC

Number of Charged Particles/bx/cm²

At SLHC we expect:

<table>
<thead>
<tr>
<th>Occupancy</th>
</tr>
</thead>
<tbody>
<tr>
<td>(10^{35} \text{ hits/cm}^2 / 25 \text{ nsec})</td>
</tr>
<tr>
<td>17.6 at R=4 cm</td>
</tr>
<tr>
<td>7.6 at R=7 cm</td>
</tr>
<tr>
<td>4.6 at R=10 cm</td>
</tr>
</tbody>
</table>

- The rate is dominated by particles with momentum below 1 GeV.
- These move helix-trajectories around the beam axis.

- Expected data rates from the Inner tracker are very large resulting to ~10¹ TBytes/sec/cm²
- This rate needs to be reduced on the detector.
- 90% of the rate comes from particles below 1 GeV in Pt
Using Tracking Information for Triggering

Electron/Photon Triggers

• Electron Triggers:
  – A factor of 10 reduction using hits in the pixels
  – A factor of 3 using the outer tracker
Using Tracking Information for Triggering

**Tau and Muon Triggers with tracking**

- **Tau Trigger:**
  - Uses isolated stubs in the pixels
  - A factor of 10 in QCD jet rejection

- **Muon Trigger:**
  - Outer tracker
  - Large rejection

### Efficiency for QCD events

![Efficiency plot](image)

<table>
<thead>
<tr>
<th>Level</th>
<th>Single</th>
<th>Double</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level-1</td>
<td>6200</td>
<td>1700</td>
</tr>
<tr>
<td>Level-2</td>
<td>700</td>
<td>35</td>
</tr>
<tr>
<td>Calo isolation</td>
<td>590</td>
<td>25</td>
</tr>
<tr>
<td>Level-3</td>
<td>100</td>
<td>10</td>
</tr>
<tr>
<td>Level-3+calo tracker isolation</td>
<td>50</td>
<td>5</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>55</td>
</tr>
</tbody>
</table>

\[
\text{Rate (Hz)} = L \times 10^{34} \text{cm}^2 \cdot \text{s}^{-1}
\]
2D Short Strip - Time Walk

- Measure the time delay between the charge injection and detection (fast OR) Convert the voltage to amount of charge assuming the design capacitance of the charge injection capacitors
- Vary the preamp bias voltage to adjust the front end bias current

The graph shows the delay from injection to discriminator output (ns) as a function of injected charge (fC) with different currents (4uA, 8uA, 16uA, 20uA). The equation $a + bx^{-c}$ is used to model the data.
Simplified Functional View of CMS Demonstrator Chip
Why Did 3D Fab Take So Long?

- **Design Issues**
  - Everyone did not use the same design kit provided by Tezzaron. Some design rules were interpreted incorrectly leading to various TSV design problems.
  - Initially some designs did not use a fill program resulting in fill problems later on
  - The bond pad interface pattern must be uniform across a reticule. Repeated requests to route on the bond layer had to be denied.
  - SRAM cells raised numerous questions.
  - MicroMagic software issues.

- **Submission Issues**
  - After designs were completed Chartered requested additional street space. It took three submissions before Chartered would finally accept the frame.
  - Individual blocks were incorrectly mirrored by the mask house
  - Chartered would not accept some error waivers we thought were acceptable.
  - Some designs were submitted with incorrect mirroring

- **Fabrication Issues**
  - 3D fabrication done in Chartered prototype line
  - Chartered was bought by Global Foundries which slowed our wafer fabrication process
  - Global/Chartered did not properly place frames on wafers for 4 different lots of wafers
  - Due to delays in fabrication, the 3D wafer bonding facilities were not available when the wafers were ready.
A: front-ends for 320 (5x64) strips
B: back-end readout architecture
C: LVDS drivers for readout output
D: DACs providing front-end bias
Each strip set contributes 8-bits to the output stream – 1 coincidence bit, 1 long strip (Φ) hit, 5 short strip (Z) hits, and a Sync Bit. These are driven off the chip serially.
How to Build – 3D Integration

thinning, alignment, oxide bonding, cu-cu bonding, through-silicon-via, ...

Flip wafer, dice and place on short strip sensor wafer

Tezzaron Wafer after bonding

Bulk Silicon

Cu 3D connection

Tezzaron Wafers

Send to Ziptronix

Bulk Silicon

Handle Wafer

Thin to top pad side TSVs

Oxide bond to handle wafer at Ziptronix

Thin to sensor side TSV at Tezzaron or Ziptronix

Sensor Wafer

DBI Bond to sensor wafer

Grind and etch to TSV, metalize

Dice
First Prototype ROIC - VICTR

- Two tiers vertically (3D) integrated with Cu-Cu bonding:
  - Frontend signal amplification, shaping and discrimination for top and bottom sensors done separately in the top and bottom tiers.
  - Transfer discriminator output from the top to the bottom tier and form a simple top/bottom coincidence for each set of 1 long top strip and 5 short bottom strips with the same Φ value.
  - Expect considerable increase in complexity as we move towards the final design, such as the incorporation of neighbor hits into the coincidence detection circuitry.

Top Pads deposited after thinning

Copper bonding array, 8 μm pitch

Through silicon-via
VICTR Test Stand

- Two customized PCB boards (passive components+LVDS/CMOS drivers).
- National Instruments FlexRIO system (PC, on-board FPGA module, LVDS I/O adapter module) and Labview.
Discriminator threshold for each strip can be controlled independently, allowing for a reduction in the dispersion of the threshold voltages among the strips. Width goes from 12 to 3 mV (to 1 mV after second round).
2D Short Strip - Cross Talk

- Found digital to analog crosstalk for specific channels
- We find that within a strip set, if Z<0> has a lower threshold than Z<1-4> and if it is activated at the same time, then the turn-on curve of Z<1-4> becomes like Z<0>’s
- Does not matter if interposing strips are killed or not
2D Short Strip – Cross Talk

- In each strip set, the 5 discriminator output lines run the same distance to achieve the same capacitance.
- This means the $Z<0>$ line runs past each of the sensor pads, 10 microns away.
- Induces charge in the subsequent front ends causing lower thresholds.

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Active Edge Silicon Sensor

• p+ diodes on n bulk ($\rho=5k\Omega\cdot\text{cm}$)
• 50 $\mu$m deep n++ trench at the edge
  – can use it as a high quality detector edge
  – can use it as an electrode – eliminating edge losses in tiling reticle-sized detectors
• masks designed at Fermilab
• fabricated by MIT-Lincoln Lab
Active Edge Silicon Sensor

Top view of the pixel array. (20-micron pitch)

Array of 64 x 64 pixels
Active Edge Silicon Sensor

Sensor bias scheme:
- p+ diodes (DBI) connected to FPIX input at ground potential;
- n++ trench (DBI) connected to positive potential through FPIX.

The electrical connection from the trench to the ground surface of the backside might be either (a) along the surface and cut edge or (b) by punch-through 50 µm bulk.

(optional) n+ pinning layer surrounding p+ diodes and extended to trench:
- commonly used in optical devices to passivate the detector surface;
- could act as a shield between the detector and ROIC.
The rapid increase of the leakage current beyond the full depletion voltage is due to the bare ground backside surface and the associated crystal damages.

Have sent chips to Cornell to further thin the sensors down to 50 µm (include a fine grind process "near-CMP" quality), backside implant and laser annealing.
Inject a laser onto the sensor backside. Measure the analog outputs of two FPIX channels (A, B) close to the laser, and that of a channel (C) far way from the laser.

- Amplitude of Anal_Out of A and B increase versus bias – depletion volume increase.
- Amplitude of Anal_Out of C (interpreted as noise) decreases versus bias – input capacitance of the sensor to the FPIX pre-amplifier decreases versus bias.
- Rise time of A decreases versus bias – drifting starts to dominate over diffusion.
Spot a laser on the sensor backside. Measure the analog outputs of two FPIX channels (A, B) close to the laser, and that of a channel (C) far way from the laser.

- Amplitude of Anal_Out of A and B increase versus bias – depletion volume increase
- Amplitude of Anal_Out of C (interpreted as noise) decreases versus bias – input capacitance of the sensor to the FPIX pre-amplifier decreases versus bias
- Rise time of A and B decrease versus bias – drifting starts to dominate over diffusion
Use a variable X-ray source (metal films in front of Am-241) for absolute calibration:
- measure the (analog output) response curve by charge injection;
- measure (analog output) response to X-ray with different energies (22/32/44 keV);
- converting both of them to # of e/h pairs (to constrain injection capacitance $C_{\text{inj}}$).
Sensor Input Capacitance to FPIX2.1

Mean/RMS
66/11e-91/17 e-83/16 e-

Conversion from the test pulse size to the number of electrons done assuming 3.5fF injection capacitors. Absolute calibration underway.

ENC(e-)≈62+160*C(pF)

FPIX2 (vcrA) Simulated ENC Vs Cdet

a) with pinning layer C=0.155 pF
b) w/o pinning layer C=0.106 pF
Active Edge Silicon Sensor

Trench filled with oxide or polysilicon? (MIT-LL wafers had poly fill)