Development of a Readout System for Large Scale Time-of-Flight Systems with Picosecond Resolution

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We consider the development of a readout system for large-scale, picosecond-resolution, time-of-flight detector systems. The individual detector elements are 5 cm $\times$ 5 cm microchannel-plate photomultiplier tubes (MCP-PMTs) that detect the arrival of charged particles. A typical system for use in high-energy physics would have $\sim 10,000$ of these modules. The anode collects the charge from the MCP-PMT into four output channels. Each channel is connected to a front-end chip that makes a high-resolution time measurement relative to a reference clock. Each of the four front-end chips per module outputs an analog signal that is digitized by another custom chip, the control chip. The control chip also distributes the reference clock, handles the readout of the data by the data acquisition system, and does initialization and diagnostic functions. A block diagram of the readout system for one module is shown in Fig. 1.

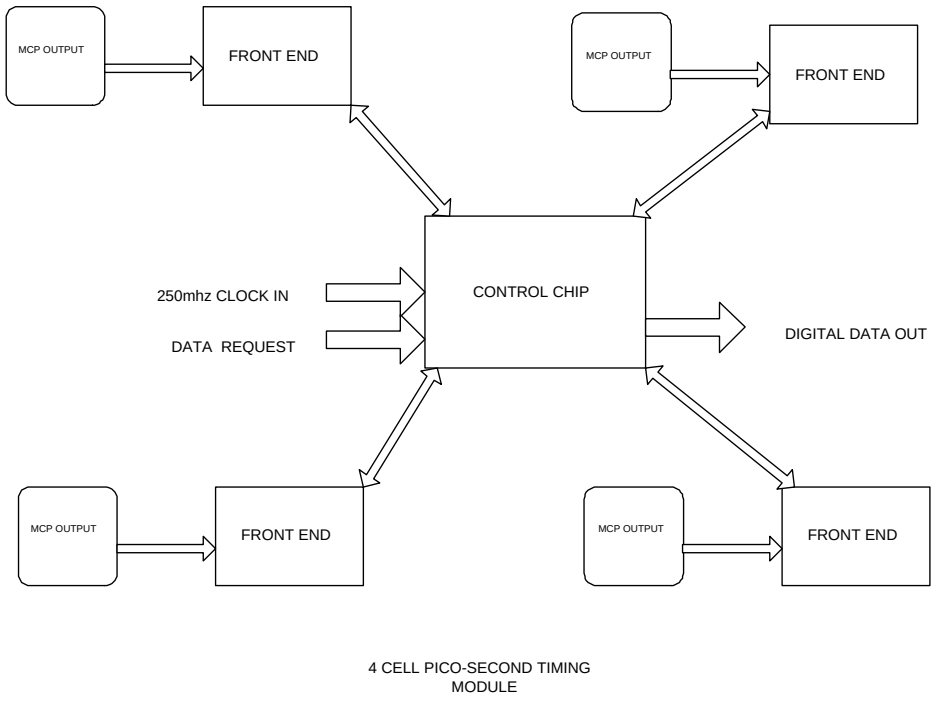

Figure 1: Readout system for an individual 5-cm by 5-cm MCP-PMT. The four front-end chips are labeled 'picosecond timing module'; the single control chip per module is in the center.

In one possible application, as a subsystem of a high-energy collider detector, the reference time would be given by a beam-crossing strobe from the accelerator. A phase-locked loop in the control chip provides a higher frequency clock derived from the system clock which serves as a reference clock for the front-end chips.

The front-end chip will have a 1 ps resolution and a 1 ns full range; it is reset at the end of this brief window by the reference clock from the control chip. The front-end chip outputs an analog voltage proportional to the time of arrival within the reset window. Each front-end chip is connected to an amplitude-to-digital converter (ADC) in the control chip.

The coarser stage of time-to-digital conversion is done entirely inside the control chip. A bank of binary counters tracks the number of system clock cycles and the number of reset signals to the front-end chips. Whenever the MCP-PMT produces a signal, the ADC output and the values held by these counters together describe the time of arrival.

A second task of the readout system is to transfer these data to a storage mechanism. Whenever a particular ADC is read, the data are stored in a first-in/first-out (FIFO) memory. A primary FIFO memory on the control chip accepts data containing a time stamp and pixel address from the FIFO serving each pixel, preventing data loss.

The modules of a detector would be arranged into many logical groups, each of which would share a data bus. Whenever the control chips of modules on a particular bus have data in their primary FIFOs, they attempt to gain control of the bus and transfer data to a bus controller.

A third task of the readout system is to provide the ability to test and calibrate an entire detector system *in situ*. To that end, the control chip can accept instructions from the data bus to inject signals of known length and time into its event processing pipeline.

To develop the design and test functionality in a user-friendly environment, we have implemented a prototype that demonstrates the main features of the control chip in an Altera EP1C20F400C7 Field-Programmable Gate Array (FPGA). The FPGA design assumes a Wilkinson-type time stretcher as its input. We expect to design and fabricate the control chip in the IHP SH25H2 process which includes CMOS and very high frequency SiGe bipolar transistors.