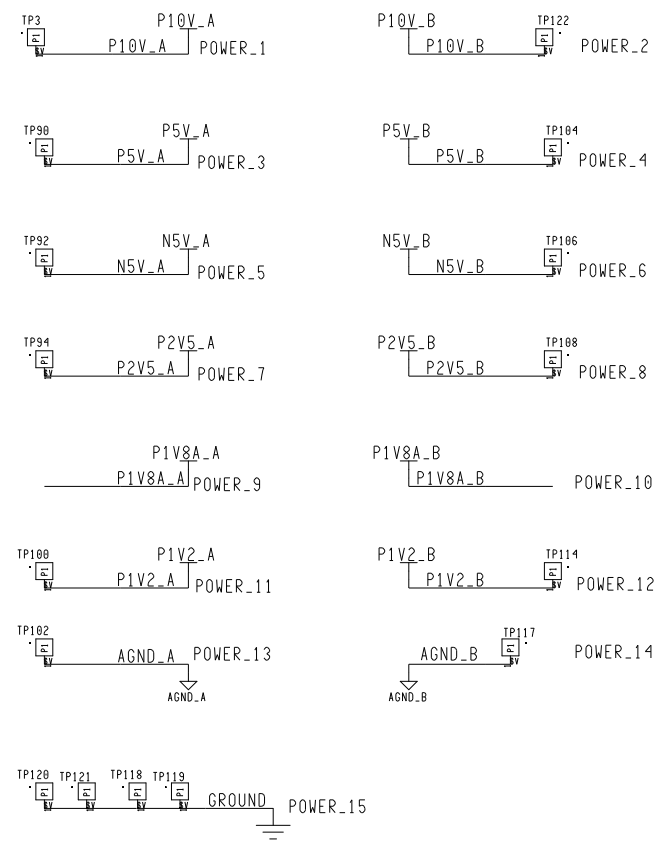


POWER_LAYERS:

- POWER-1 & POWER_2 & POWER_3 & POWER_4
- POWER_5 & POWER_6 & POWER_7 & POWER_8
- POWER_9 & POWER_10 & POWER_11 & POWER_12
- POWER_13 & POWER_14
- POWER_15



SCH#: B-2799
 SPC#: B-2800
 ASM#: B-2801

Total Sheet Number X=25

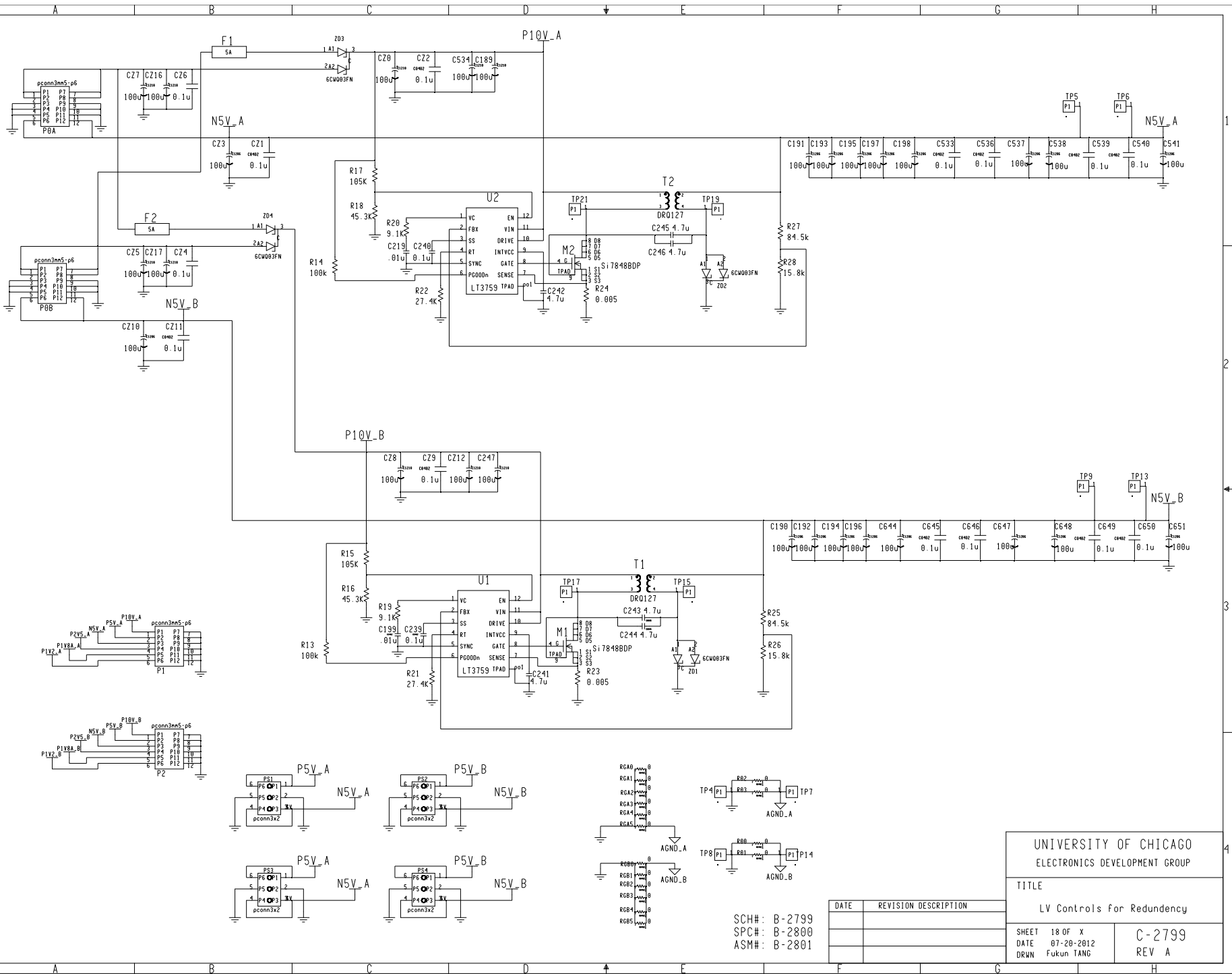
DATE	REVISION	DESCRIPTION

UNIVERSITY OF CHICAGO
 ELECTRONICS DEVELOPMENT GROUP

TITLE
 MAIN BOARD TOP

SHEET 1 OF X
 DATE 07-16-2012
 DRWN fong

C-2799
 REV A



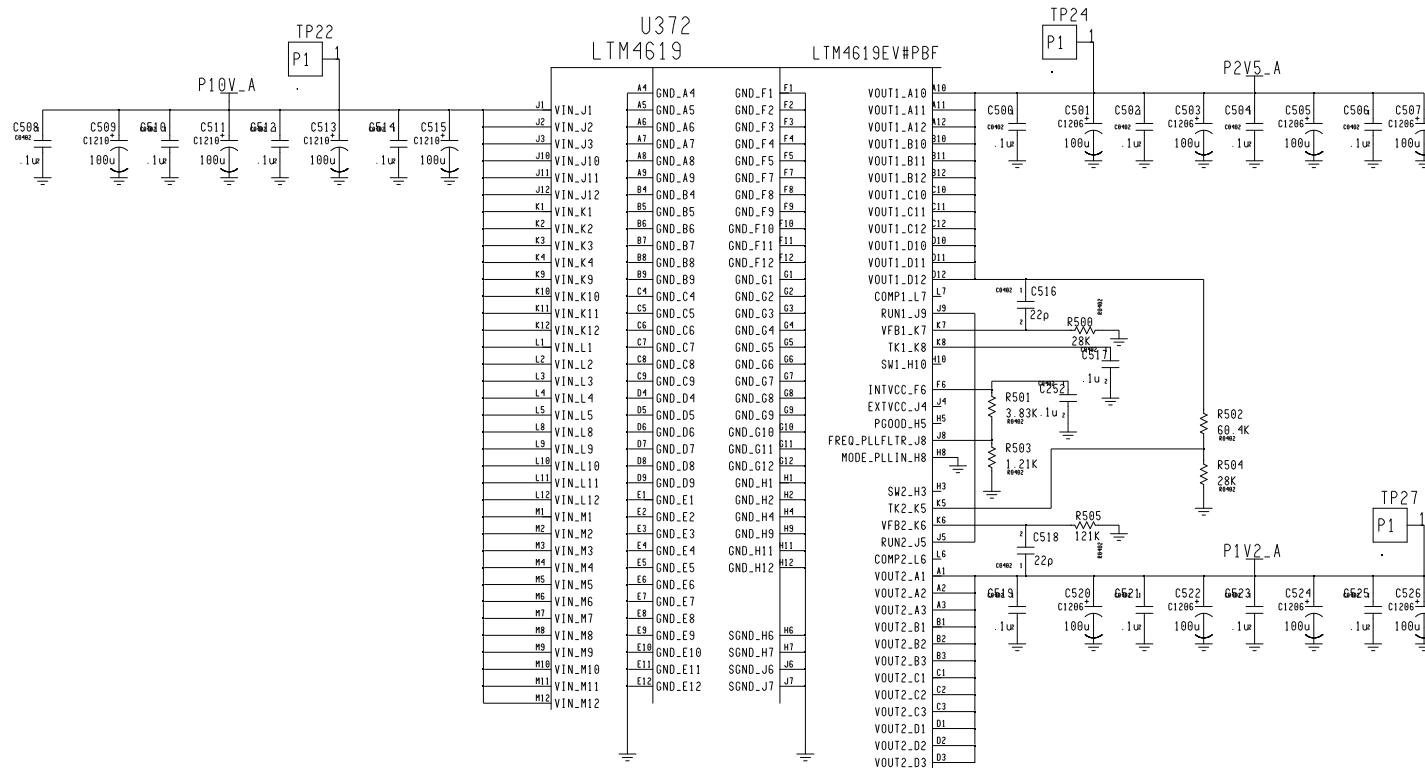
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
LV Controls for Redundancy

DATE	REVISION	DESCRIPTION

SHEET 18 OF X	C-2799
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REV A	

SCH#: B-2799
SPCM#: B-2800
ASM#: B-2801



500KHz Switcher
Synchronous ramp Up

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

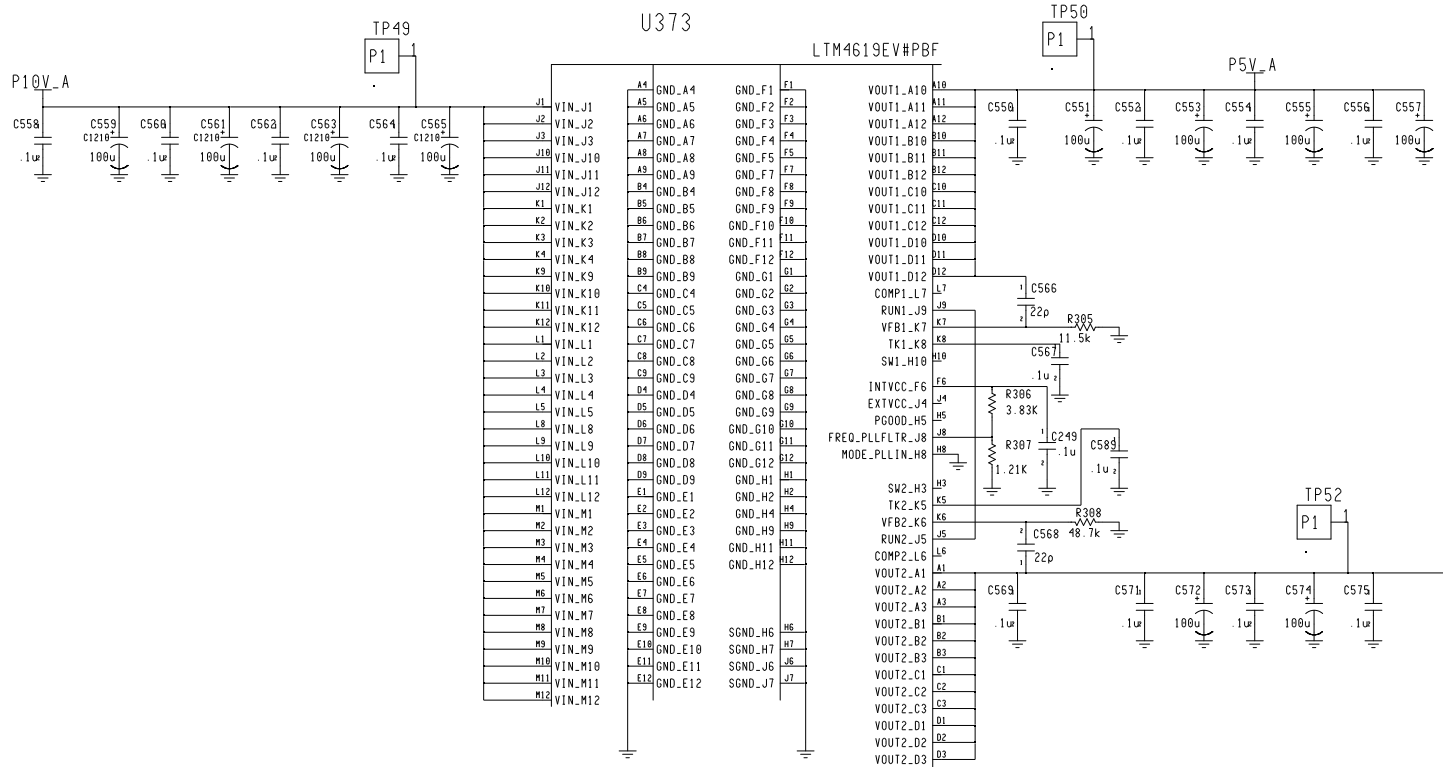
TITLE
SECTION-A: P2V5, 1V2 SUPPLIES

SCH#: B-2799
SPC#: B-2800
ASM#: B-2801

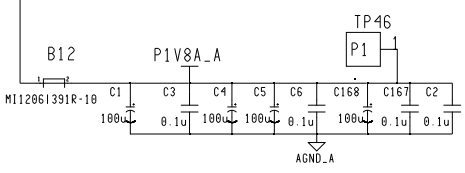
DATE	REVISION DESCRIPTION

SHEET 19 OF X
DATE 07-20-2012
DRWN Fukun TANG

C-2799
REV A



500KHz Switcher
Synchronous ramp Up



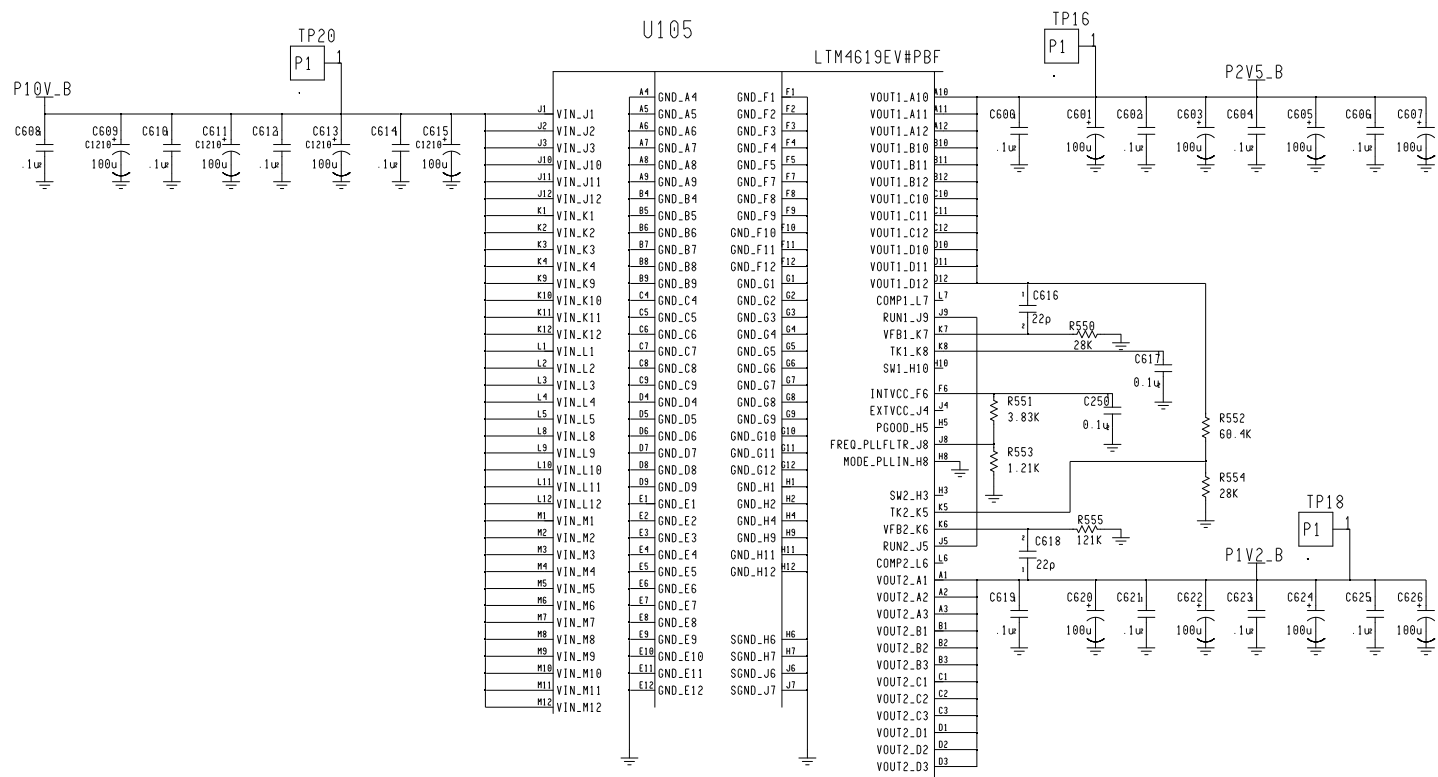
UNIVERSITY OF CHICAGO
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TITLE
SECTION-A: P5V, P1V8 SUPPLIES

DATE	REVISION	DESCRIPTION

SHEET 20 OF X	C-2799
DATE 07-20-2012	
DRWN Fukun TANG	REV A

SCH#: B-2799
SPC#: B-2800
ASM#: B-2801



500KHz Switcher
Synchronous ramp Up

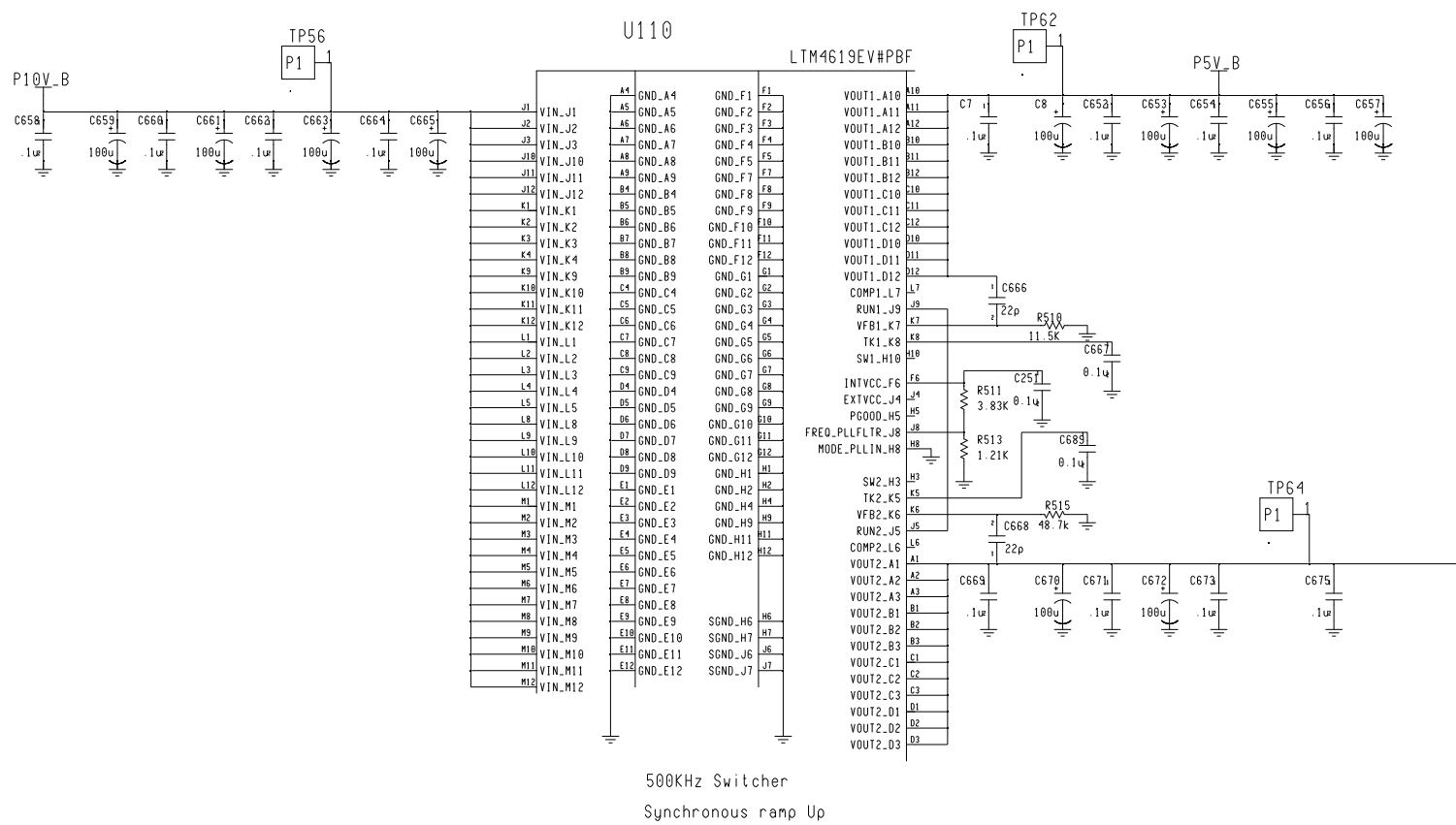
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
SECTION-B: P2V5, P1V2 SUPPLIES

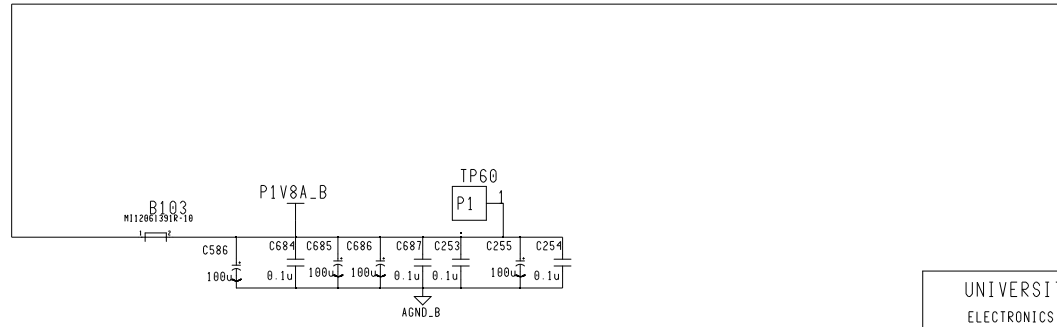
DATE	REVISION DESCRIPTION

SHEET 21 OF X	C-2799
DATE 07-20-2012	REV A
DRWN Fukun TANG	

SCH#: B-2799
SPC#: B-2800
ASM#: B-2801



500KHz Switcher
Synchronous ramp Up



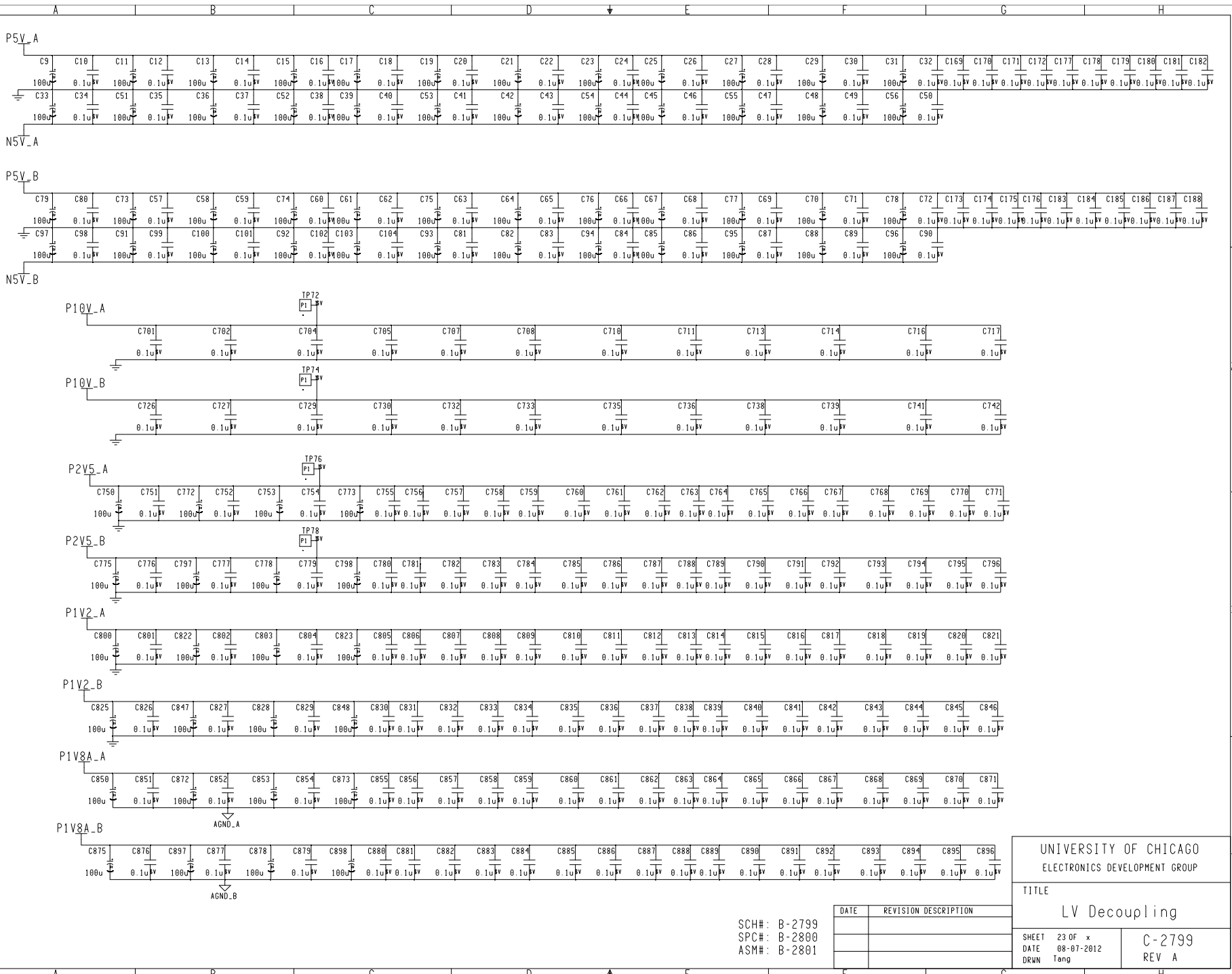
UNIVERSITY OF CHICAGO
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TITLE
SECTION-B: P2V5, P1V8 SUPPLIES

DATE	REVISION DESCRIPTION

SHEET 22 OF X	C-2799
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ASM#: B-2801



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TITLE LV Decoupling	
SHEET 23 OF x DATE 08-07-2012 DRWN fong	C-2799 REV A

SCH#: B-2799
 SPCH#: B-2800
 ASM#: B-2801

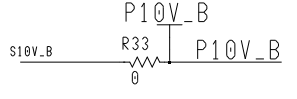
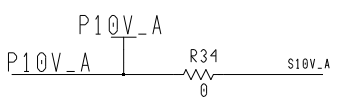
DATE	REVISION	DESCRIPTION

A

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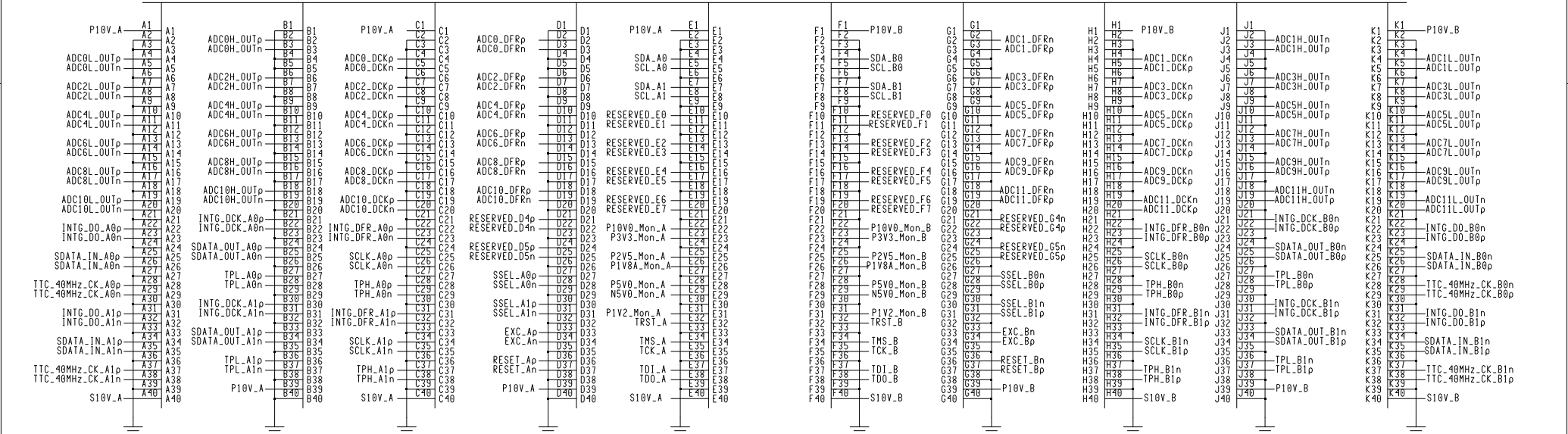
D



SAEM40x10_GP

JP0

SAEM-40-06.5-S-10-2-A



- Note-1:
- (a): RESERVED_D0p/n, D1p/n should connect FPGA-A0
 - (b): RESERVED_D2p/n, D3p/n should connect FPGA-A1
 - (c): RESERVED_D5p/n should connect FPGA-A0 and FPGA-A1
 - (d): RESERVED_G0p/n, G1p/n should connect FPGA-B0
 - (e): RESERVED_G2p/n, G3p/n should connect FPGA-B1
 - (f): RESERVED_G5p/n should connect FPGA-B0 and FPGA-B1
 - (g): RESERVED_E0, E1, E2, E3 should connect FPGA-A0
 - (h): RESERVED_E4, E5, E6, E7 should connect FPGA-A1
 - (j): RESERVED_E8 should connect FPGA-A0 and FPGA-A1
 - (k): RESERVED_F0, F1, F2, F3 should connect FPGA-B0
 - (m): RESERVED_F4, F5, F6, F7 should connect FPGA-B1
 - (n): RESERVE_F8 should connect FPGA-B0 and FPGA-B1

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TITLE
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SCH#: B-2799
SPC#: B-2800
ASM#: B-2801

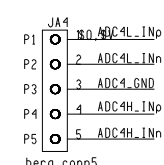
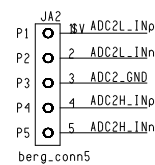
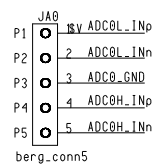
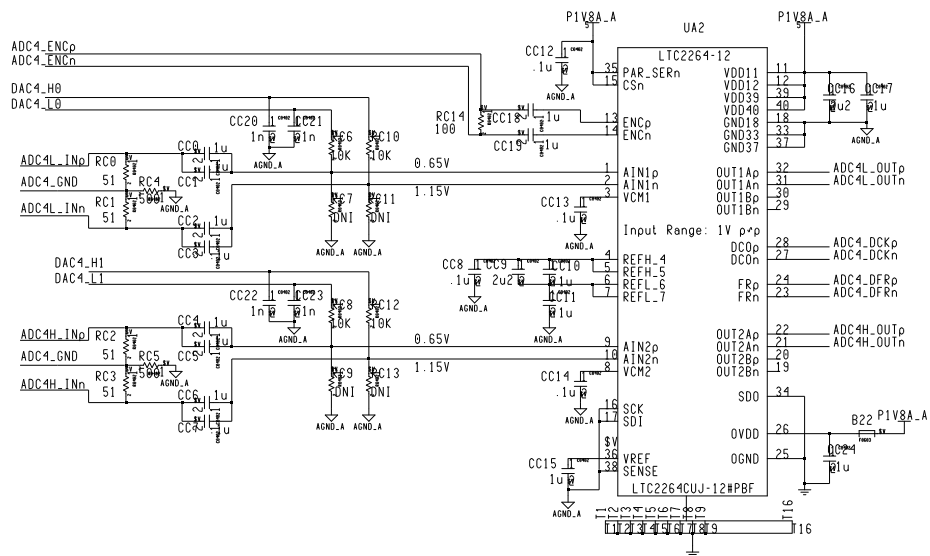
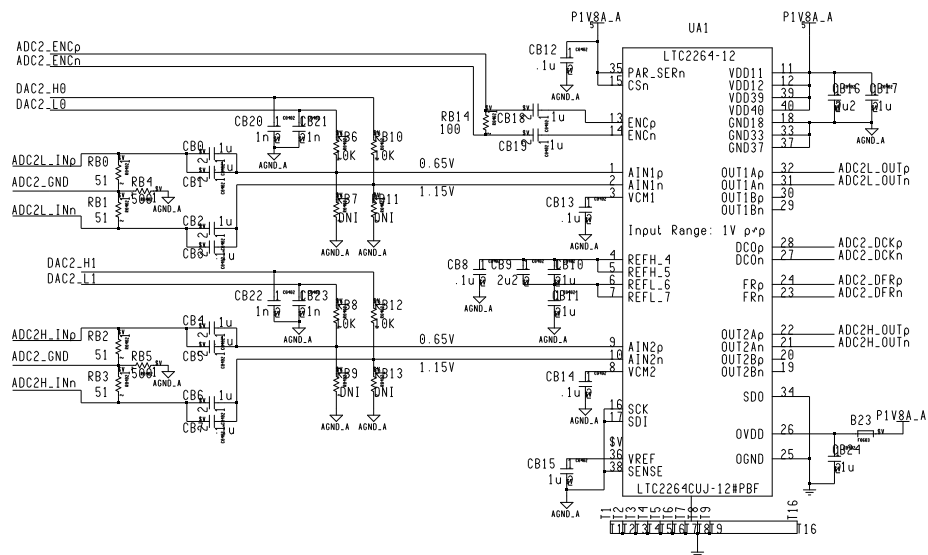
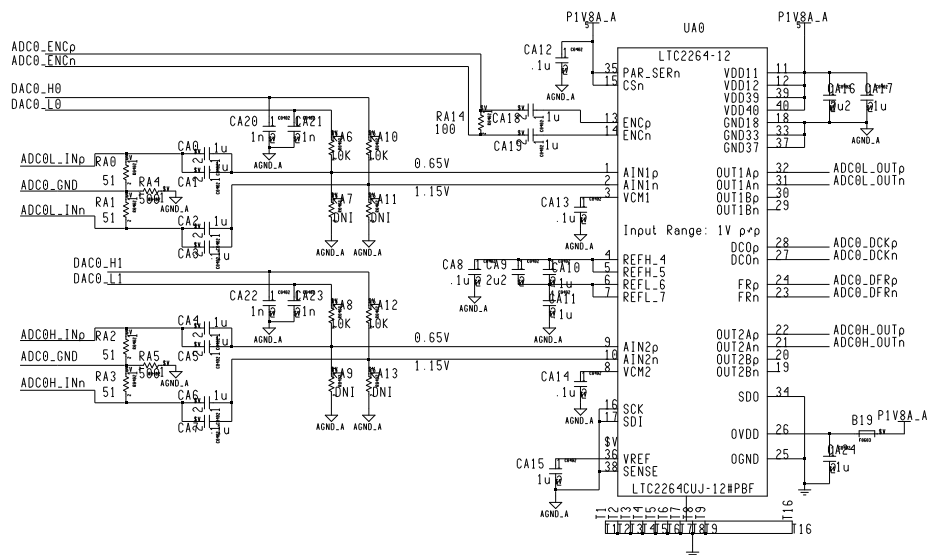
DATE	REVISION DESCRIPTION

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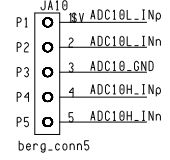
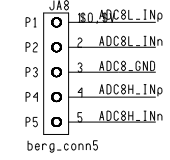
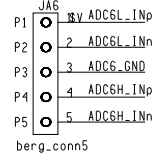
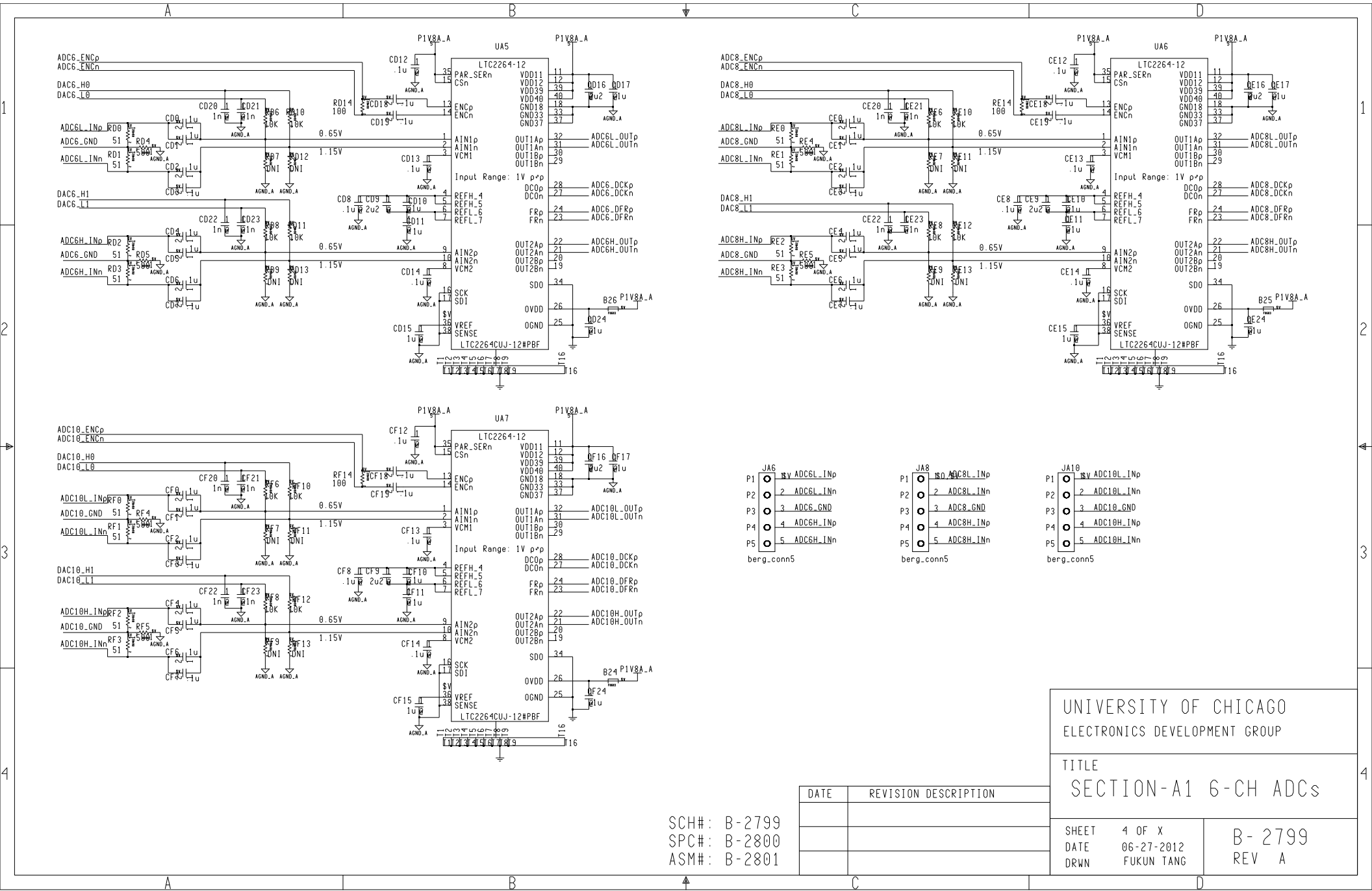
TITLE
SECTION-A0 6-CH ADCs

DATE	REVISION DESCRIPTION

SCH#: B-2799
SPC#: B-2800
ASM#: B-2801

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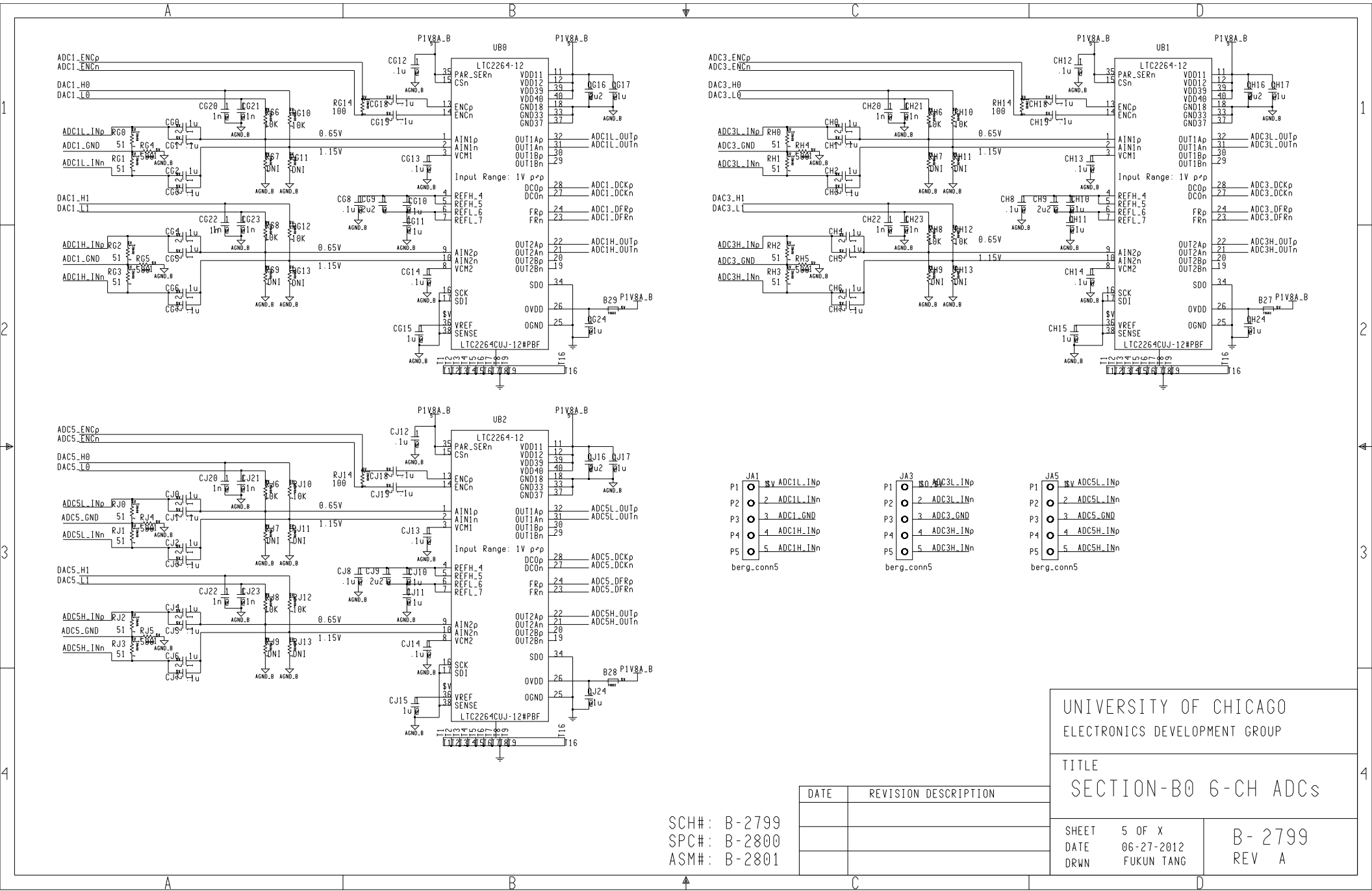
UNIVERSITY OF CHICAGO
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TITLE
SECTION-A1 6-CH ADCs

DATE	REVISION DESCRIPTION

SHEET 4 OF X	B-2799
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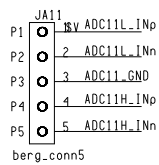
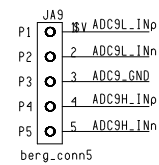
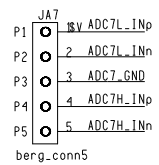
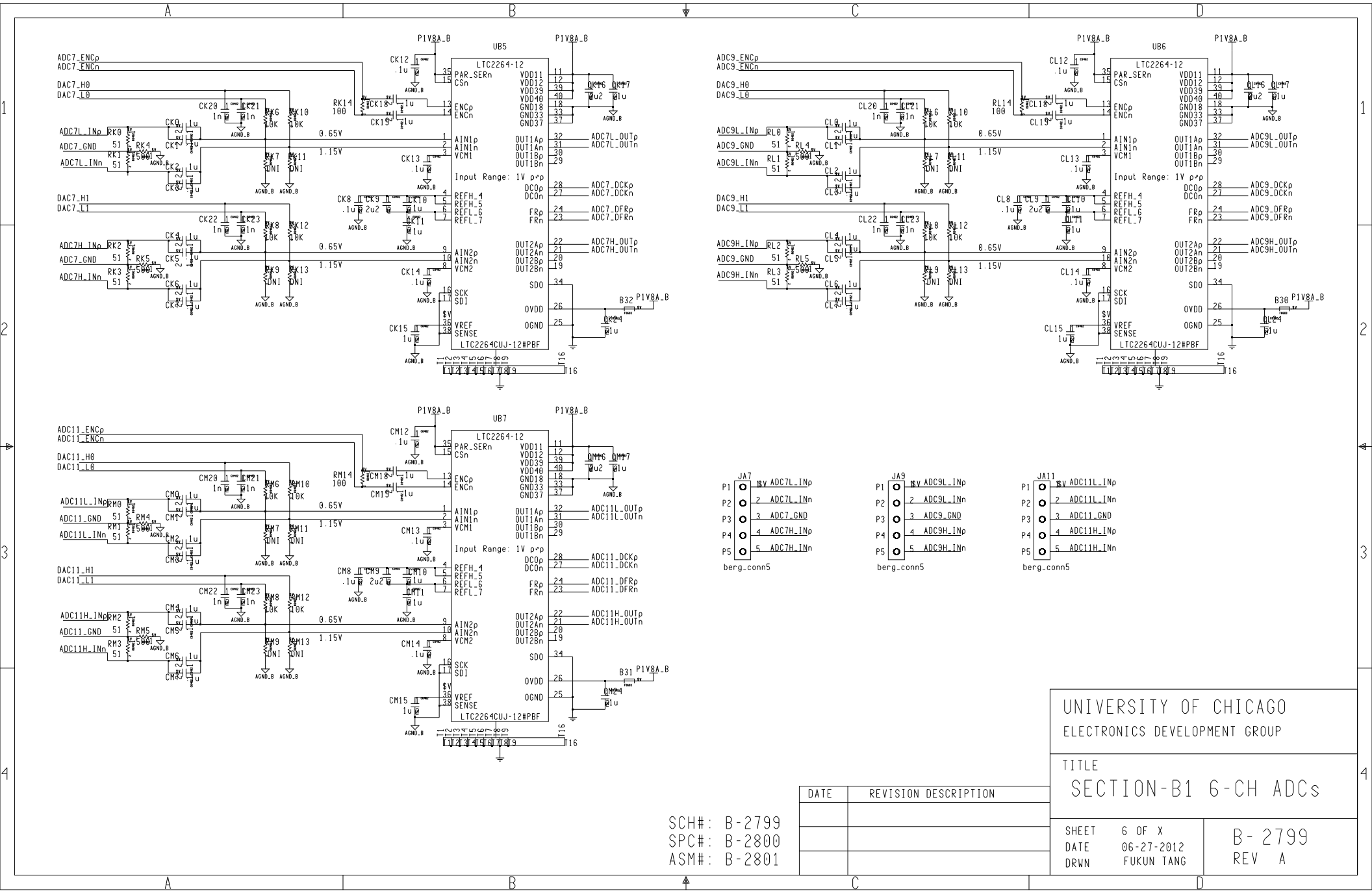
UNIVERSITY OF CHICAGO
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TITLE
SECTION-B0 6-CH ADCs

DATE	REVISION DESCRIPTION

SHEET	5 OF X	B- 2799 REV A
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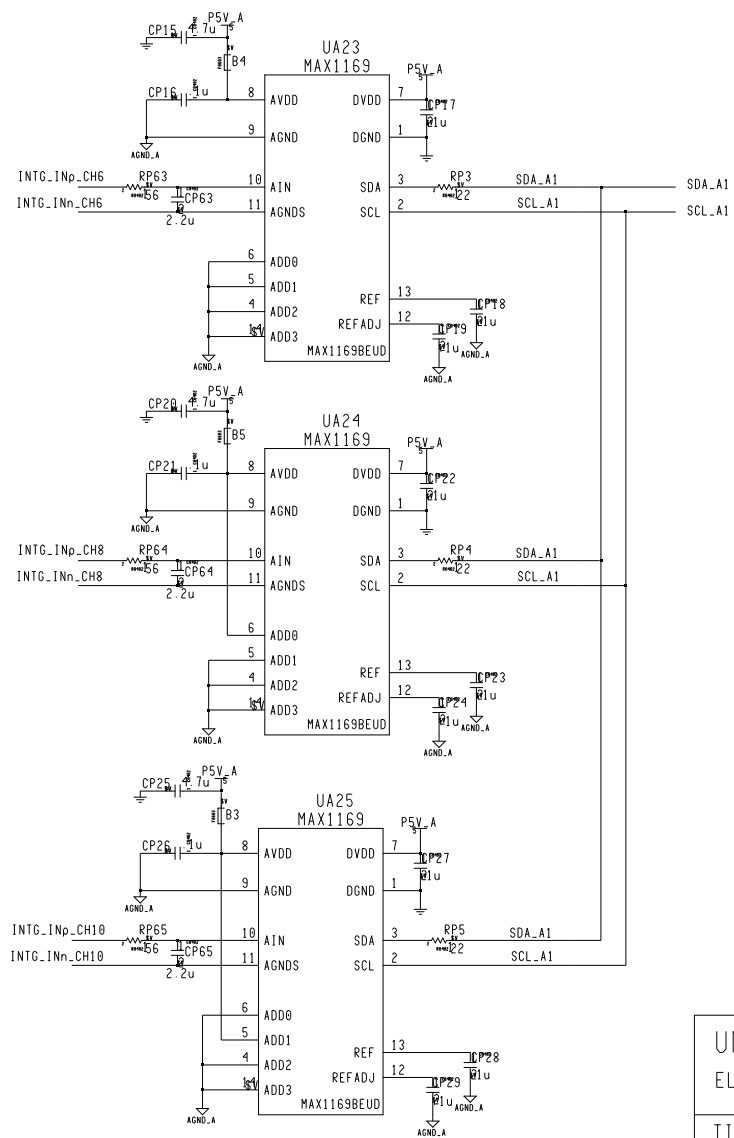
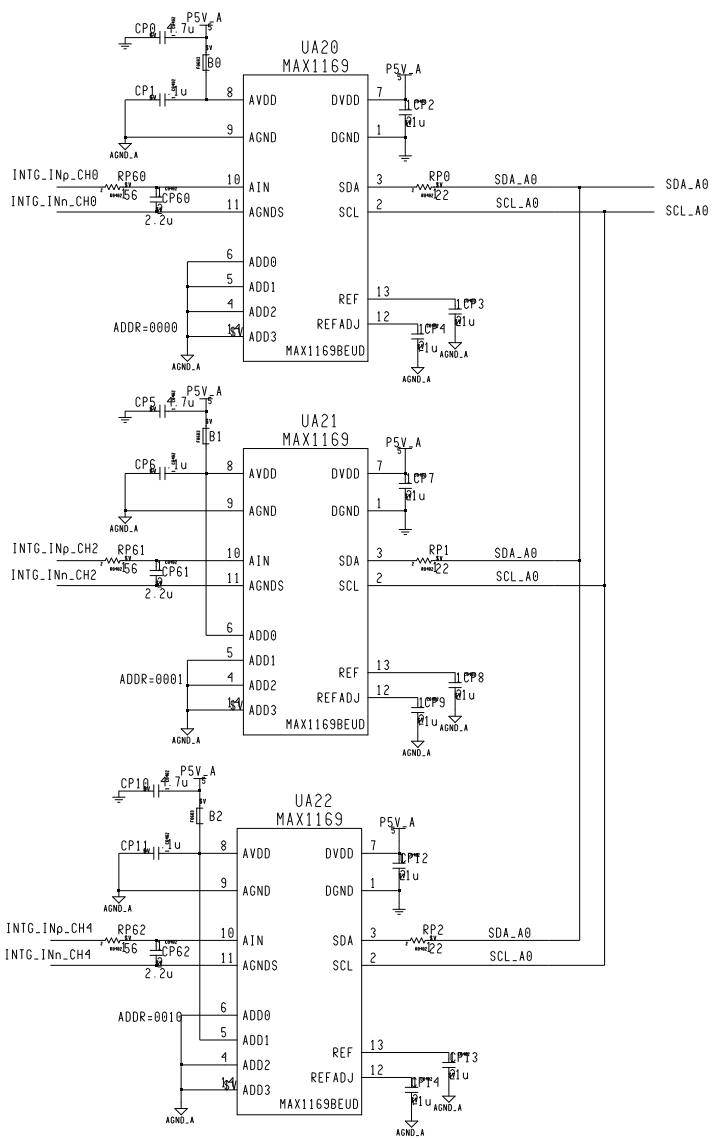
UNIVERSITY OF CHICAGO
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TITLE
SECTION-B1 6-CH ADCs

DATE	REVISION	DESCRIPTION

SHEET	6 OF X	B- 2799 REV A
DATE	06-27-2012	
DRWN	FUKUN TANG	

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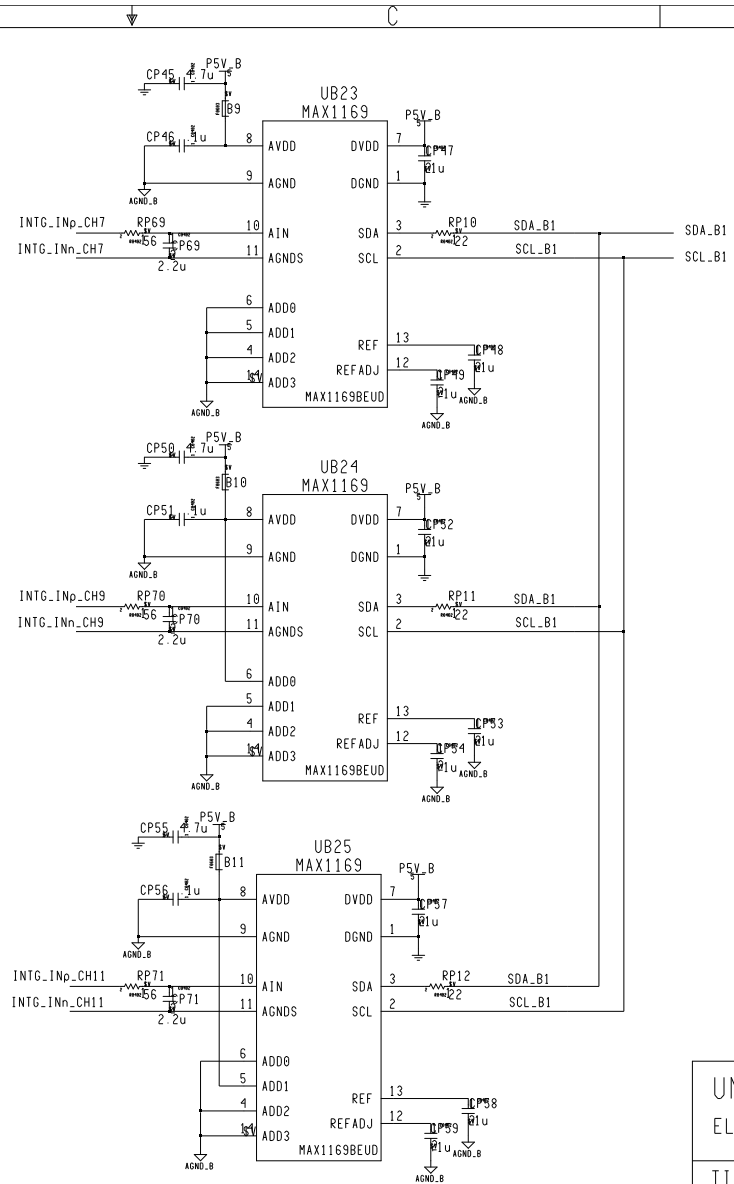
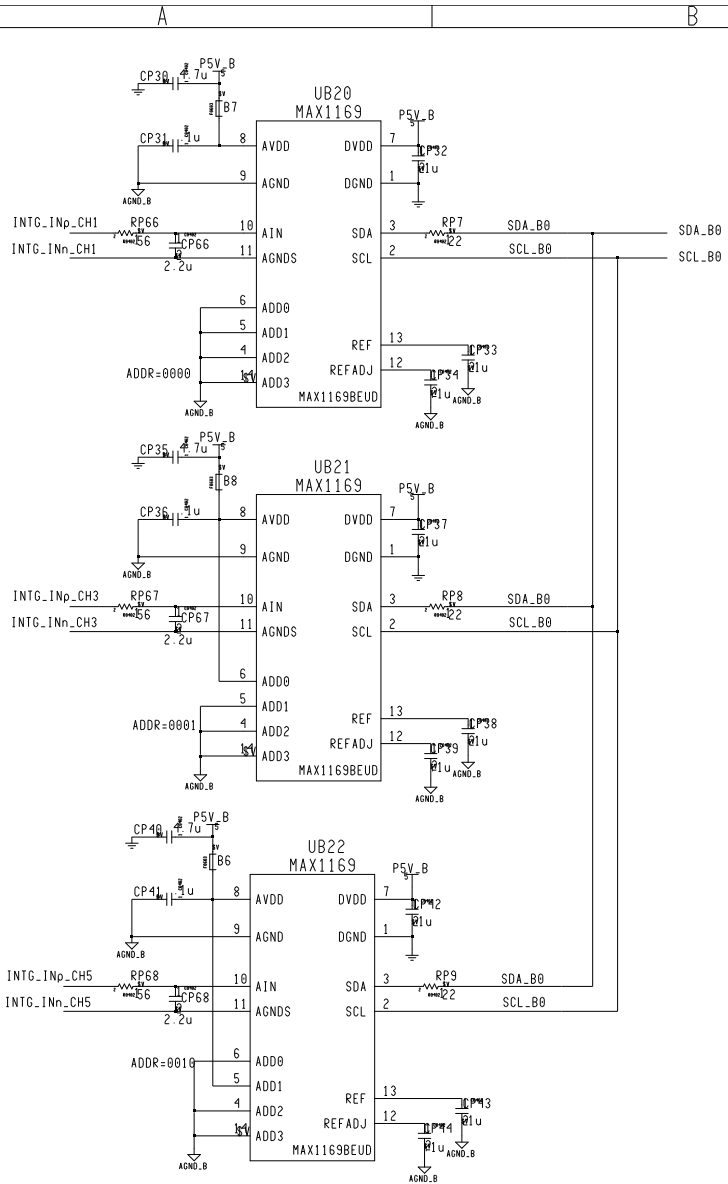
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
SECTION-A: INTEGRATOR ADCs

SCH#: B-2799
SPC#: B-2800
ASM#: B-2801

DATE	REVISION DESCRIPTION

SHEET 7 OF X	B-2799
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DRWN FUKUN TANG	



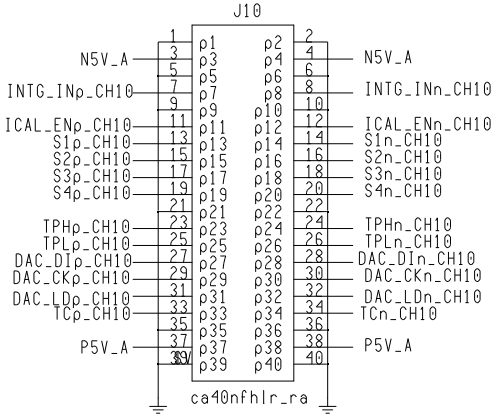
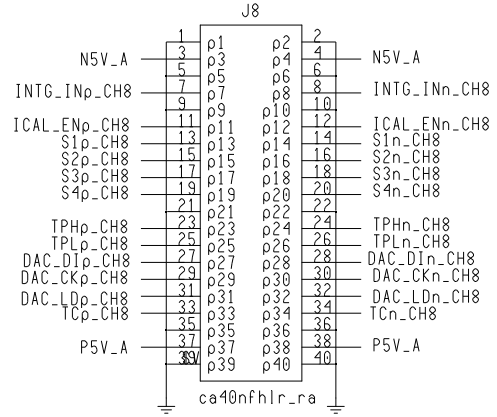
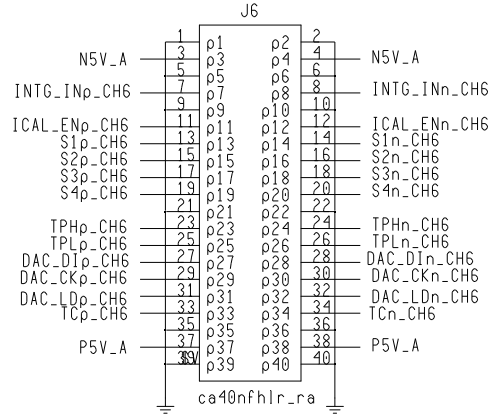
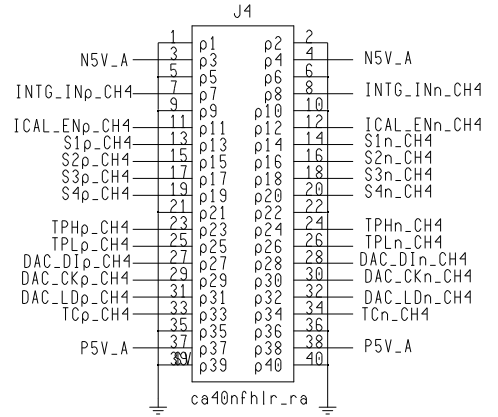
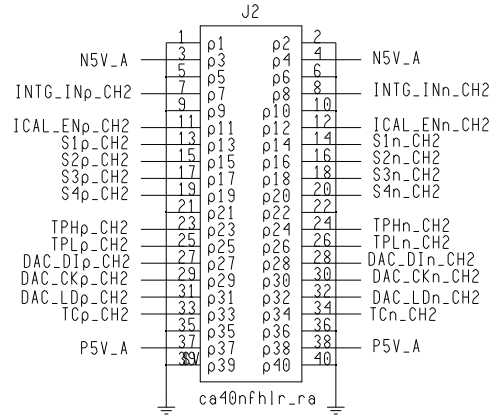
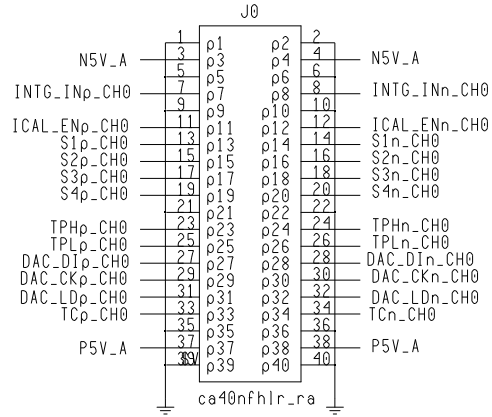
UNIVERSITY OF CHICAGO
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TITLE
SECTION-B: INTEGRATOR ADCs

SHEET	8 OF X	B-2799 REV A
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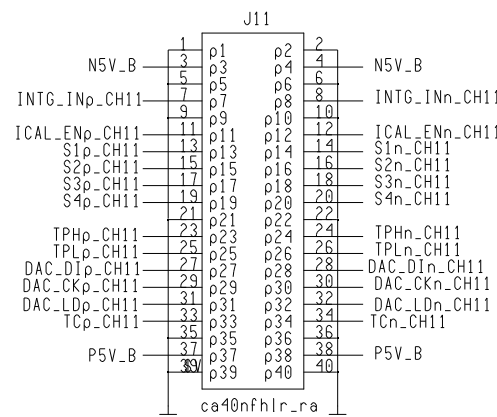
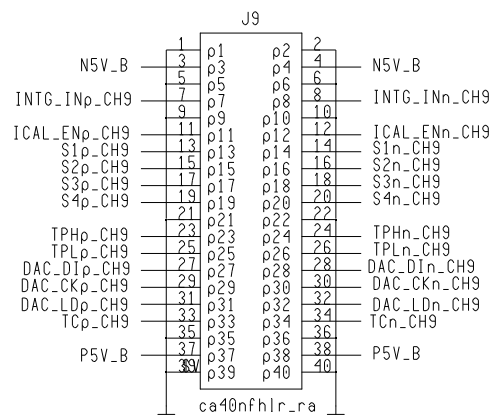
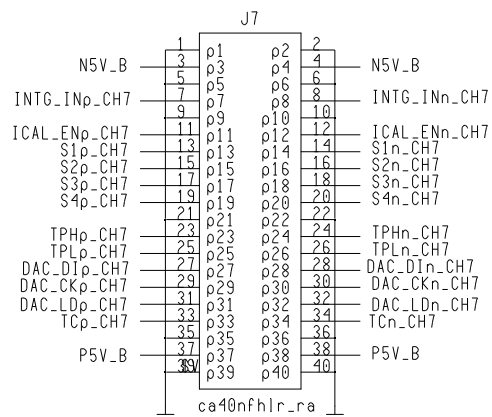
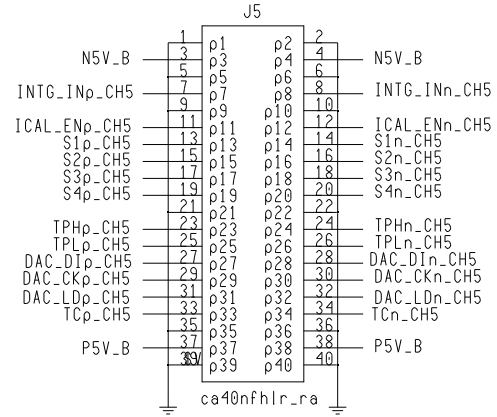
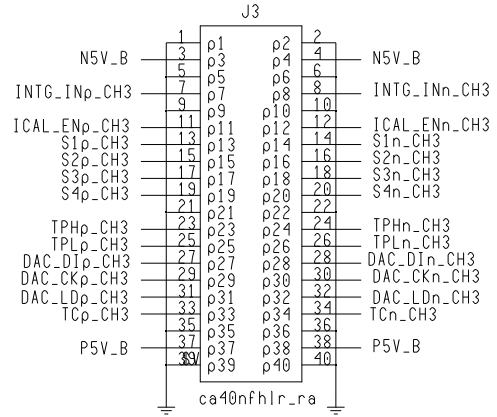
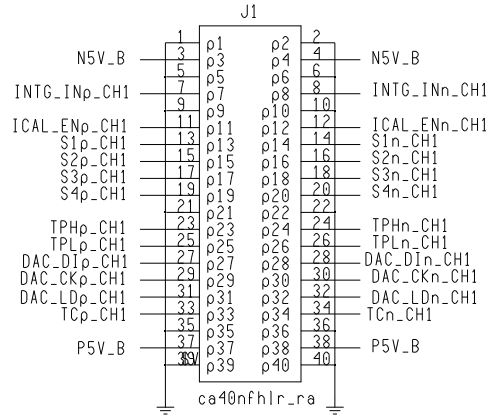
TITLE
SECTION-A: 3-in-1 PORTS

DATE	REVISION	DESCRIPTION

SHEET 9 OF x	C-2799
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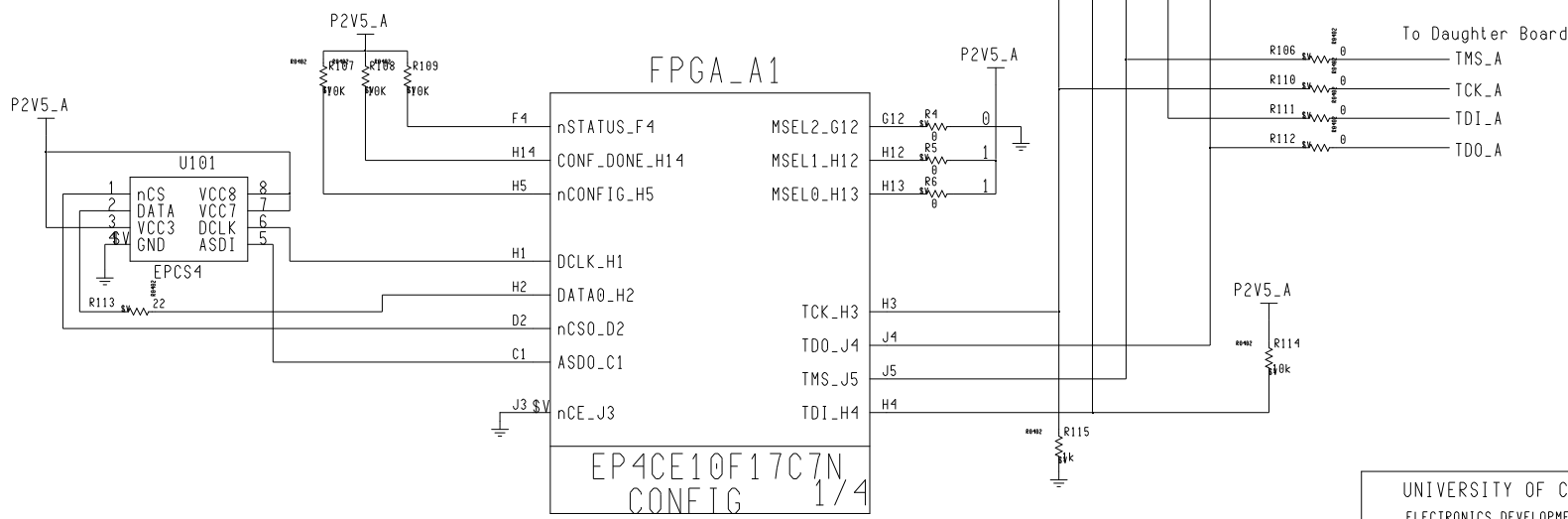
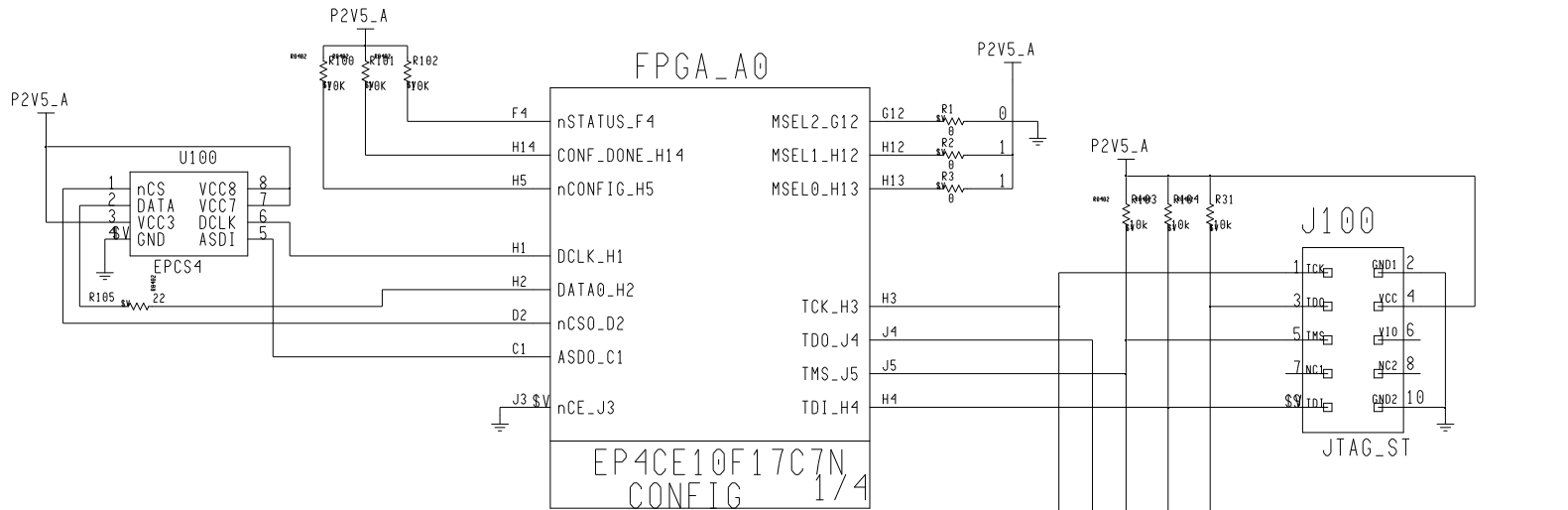
TITLE
SECTION-B: 3-in-1 PORTS

DATE	REVISION	DESCRIPTION

SHEET 10 OF x	C-2799
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SPC#: B-2800
ASM#: B-2801

A B C D E F G H



CYCLONE IV E CONFIGURATION SETTINGS

CONF	SCH#	MSEL2	MSEL1	MSEL0	CONF	VOLT
AS	1	0	1	FAST	3.3	
	0	1	0	FSF	3.0 2.5	
	0	1	1	STD	3.3	
	0	1	1	STD	3.0 2.5	

SCH#: B-2799
 SPC#: B-2800
 ASM#: B-2801

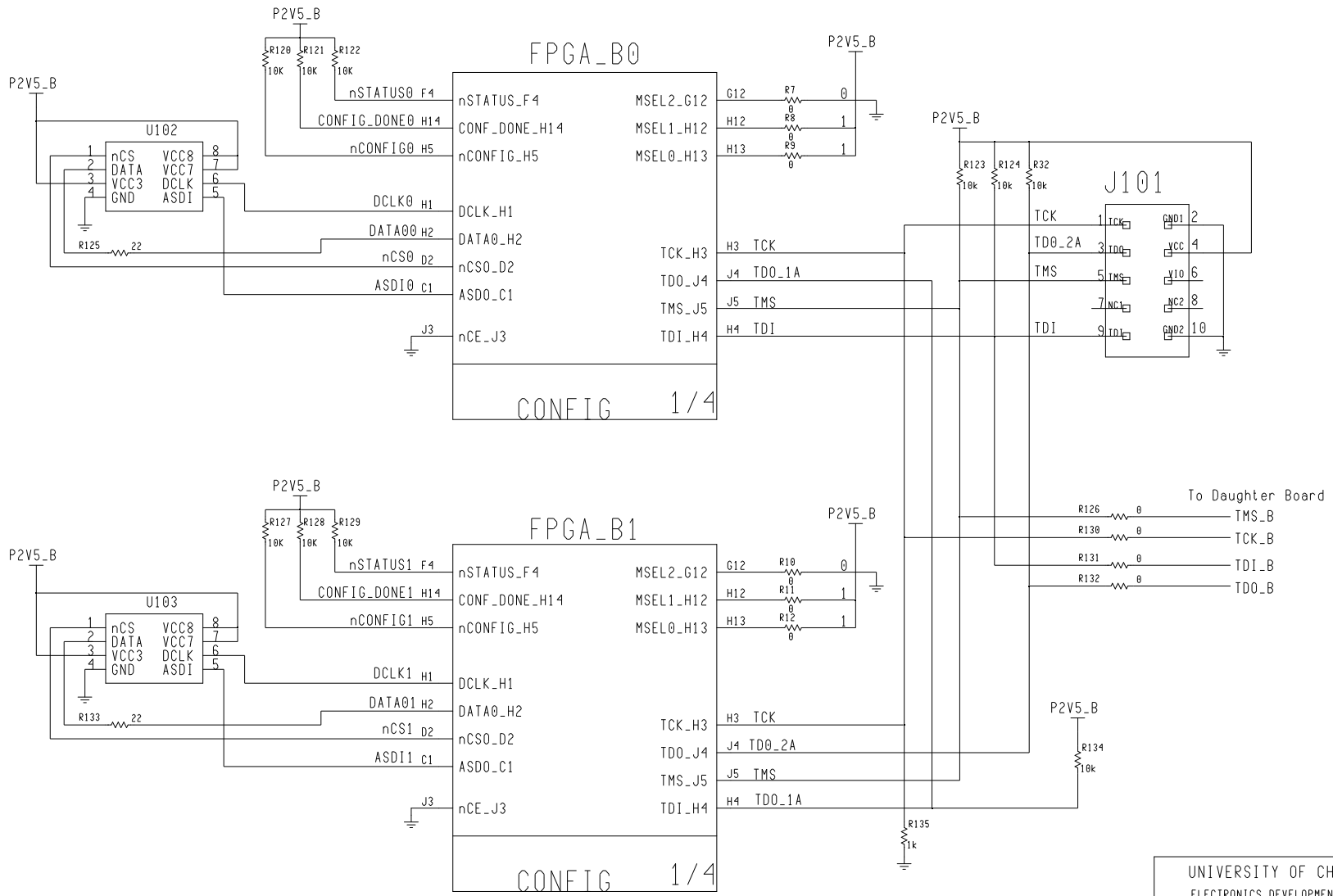
DATE	REVISION	DESCRIPTION

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TITLE
 SECTION-A: FPGA CONFIG CHAIN

SHEET 11 OF X
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CYCLONE IV E CONFIGURATION SETTINGS

CONF. SCH#	MSEL2	MSEL1	MSEL0	CONF. MOLT
AS	1	0	0	FAST 3.3
	0	1	0	FSF 3.0 2.5
	0	1	1	STD 3.3
	0	1	1	STD 3.0 2.5

SCH#: B-2799
 SPC#: B-2800
 ASM#: B-2801

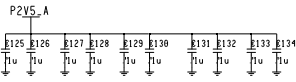
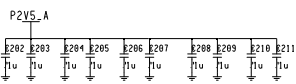
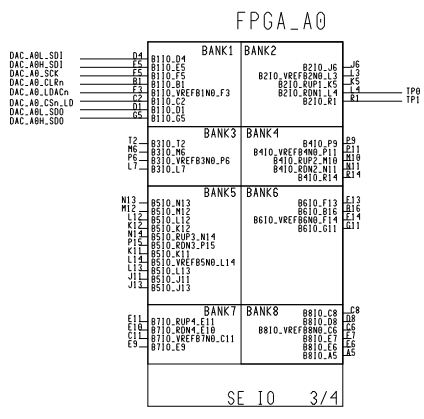
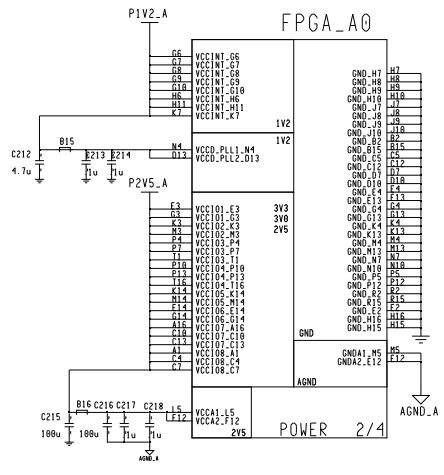
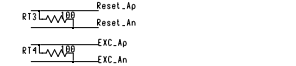
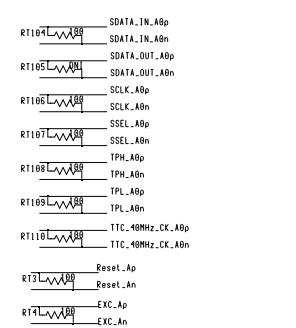
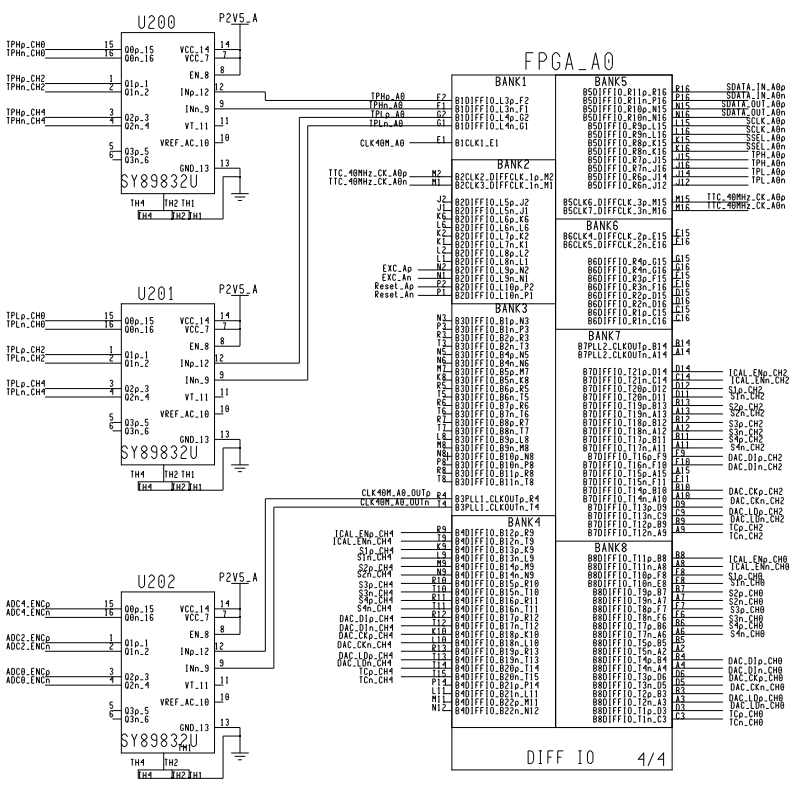
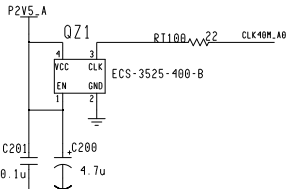
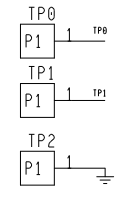
DATE	REVISION	DESCRIPTION

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 ELECTRONICS DEVELOPMENT GROUP

TITLE
 SECTION-B: FPGA CONFIG CHAIN

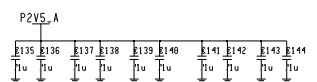
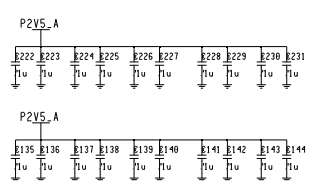
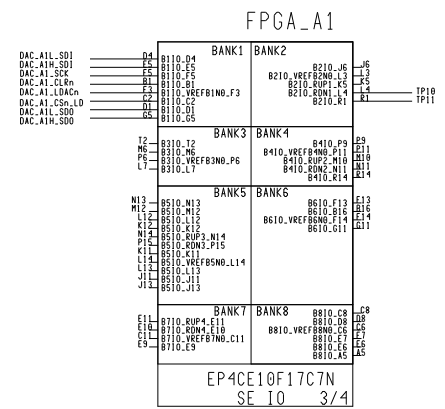
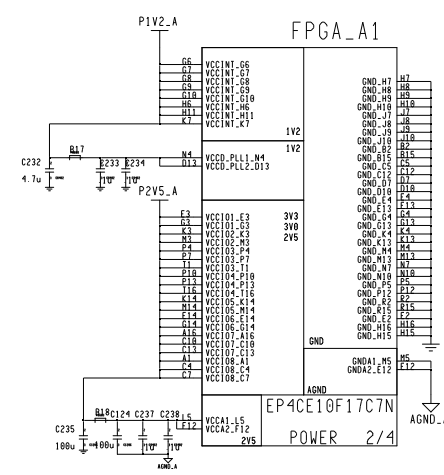
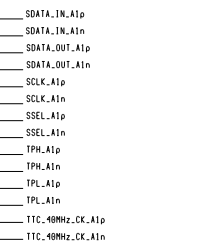
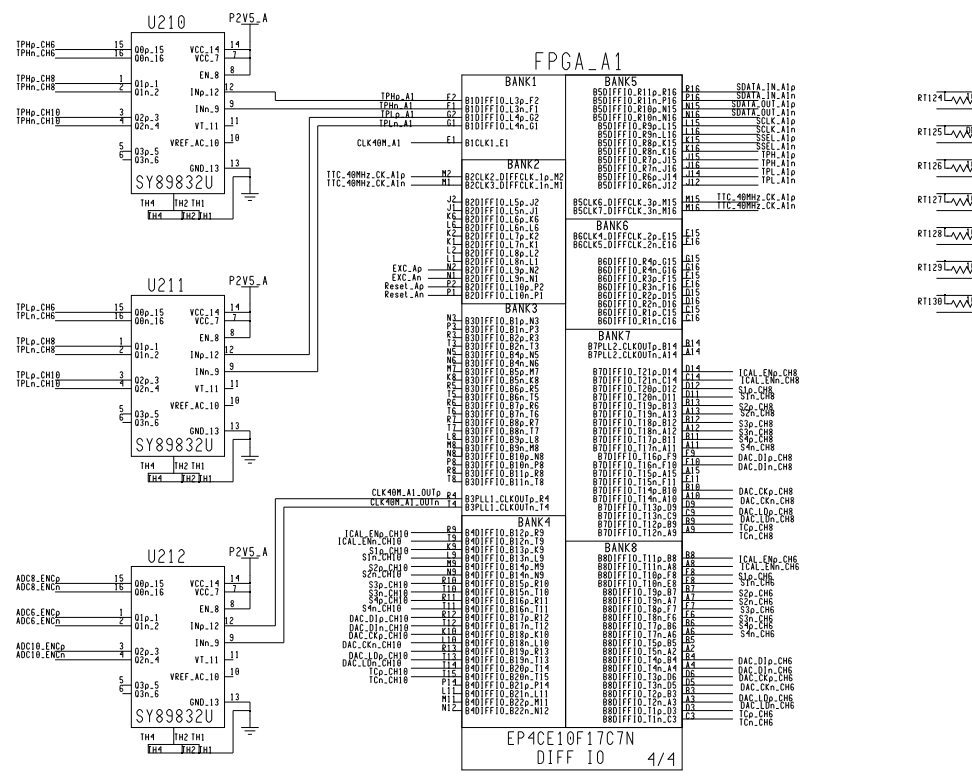
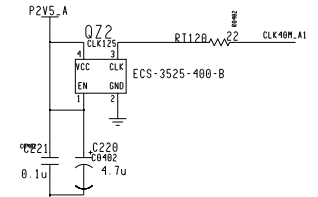
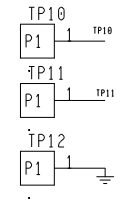
SHEET 12 OF X
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 REV A



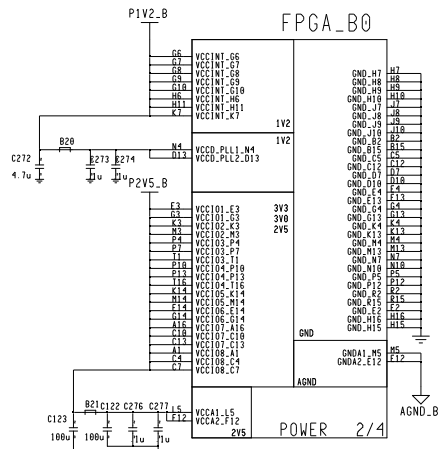
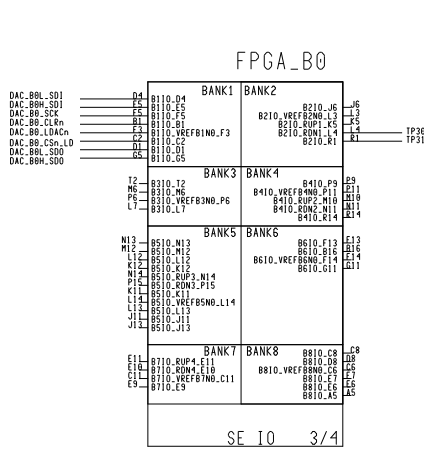
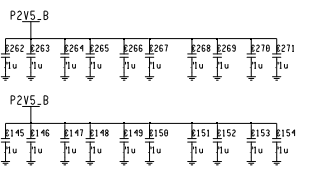
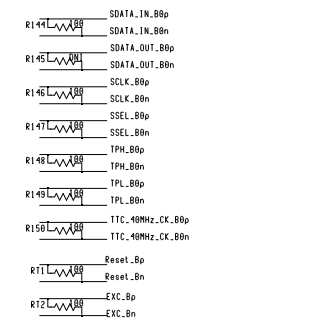
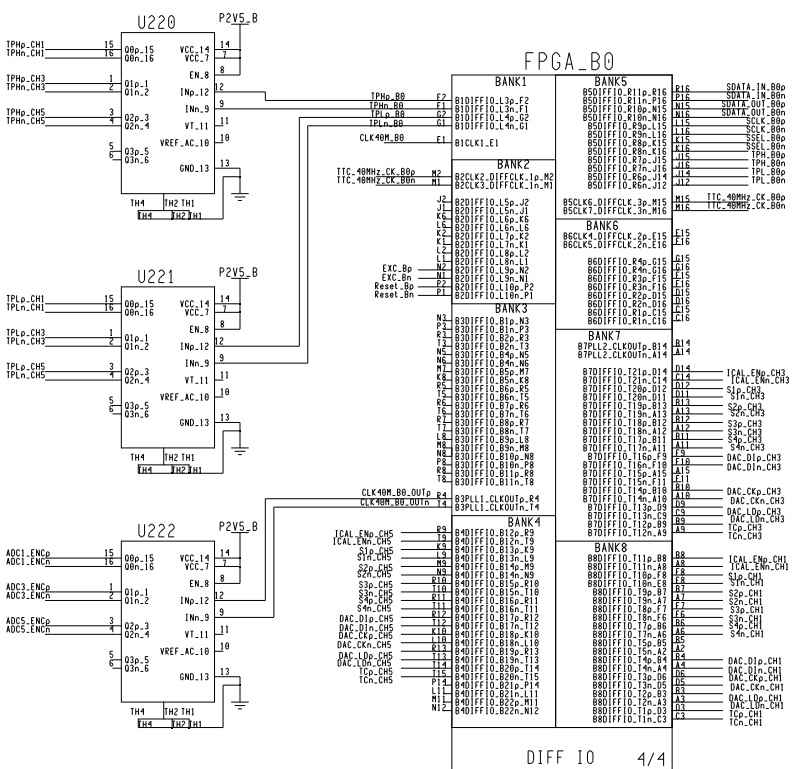
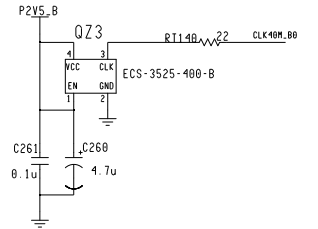
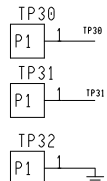
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TITLE Section-A: FPGA_A0	
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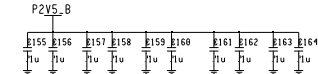
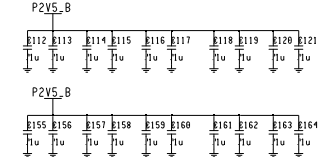
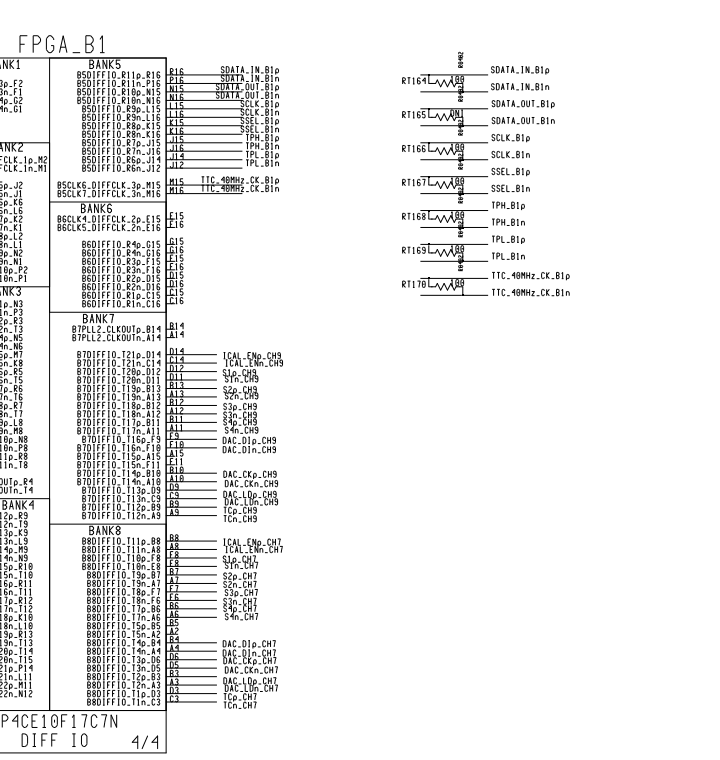
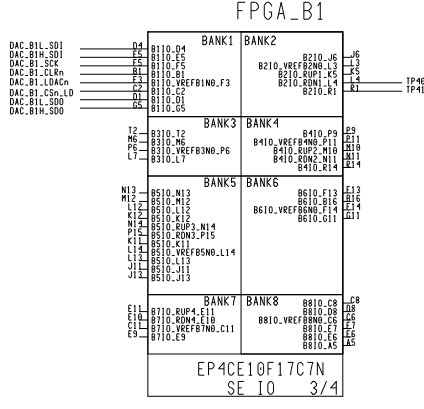
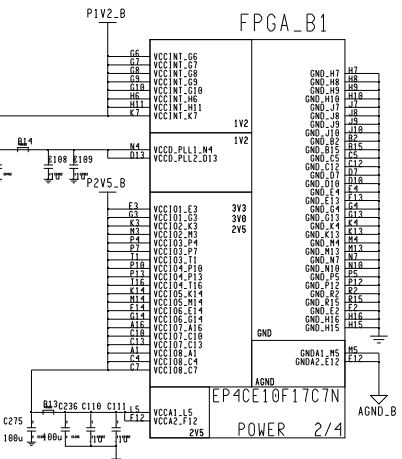
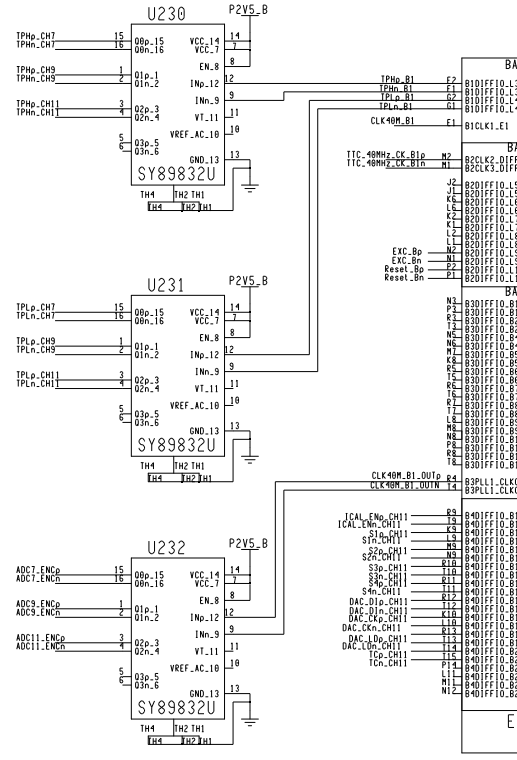
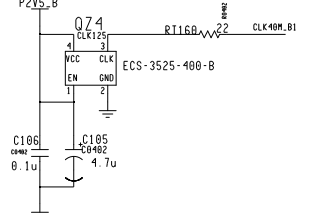
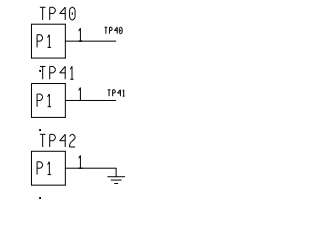


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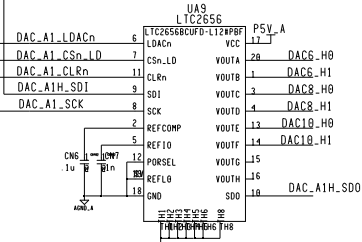
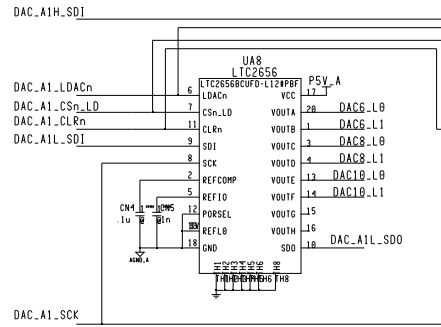
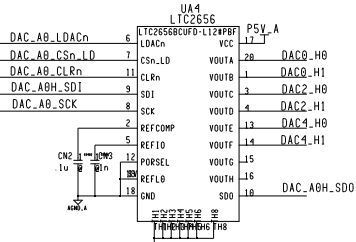
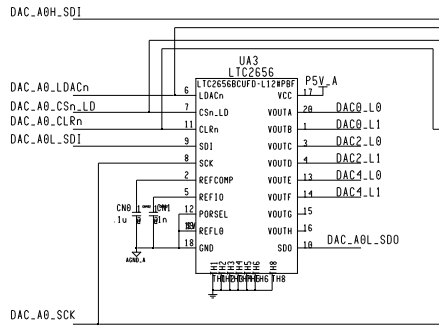
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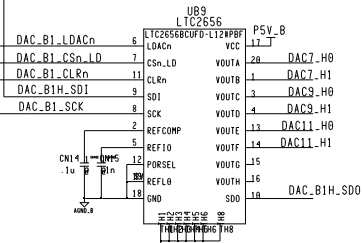
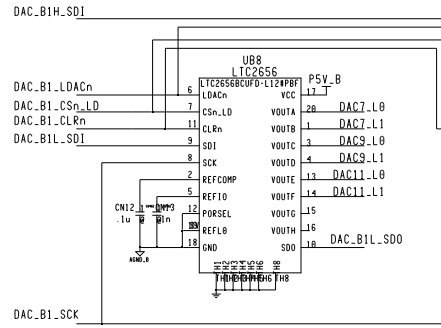
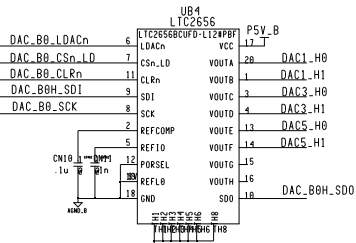
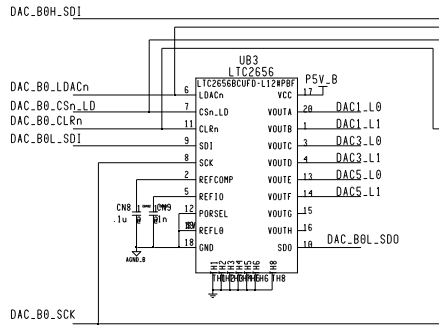
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DACs for SECTION-A



DACs for SECTION-B

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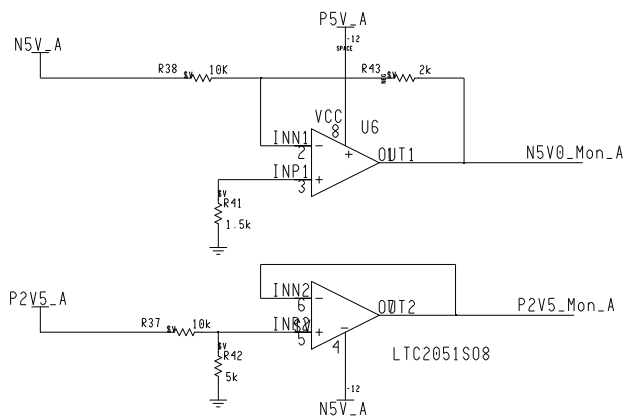
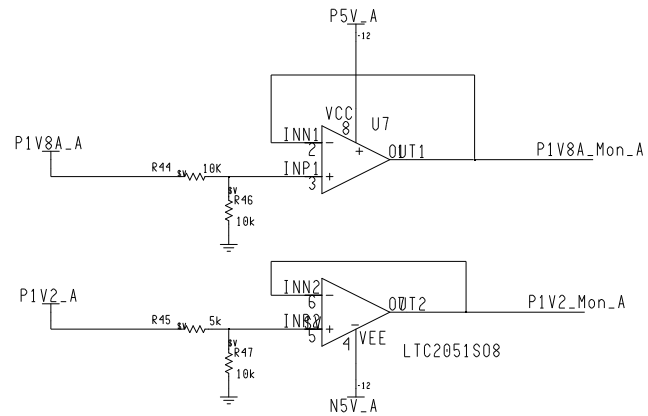
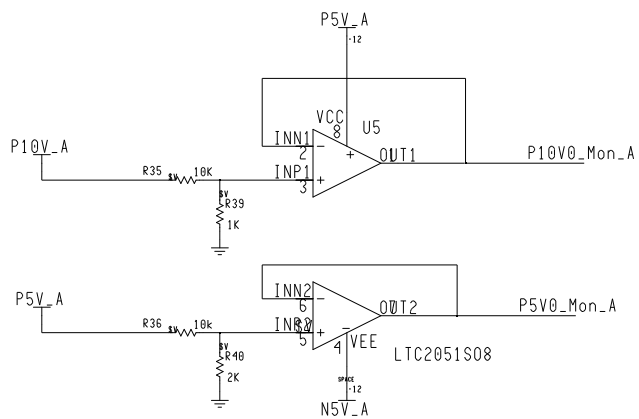
TITLE
DACs for ADC BIAS SETTINGS

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ASM#: B-2801

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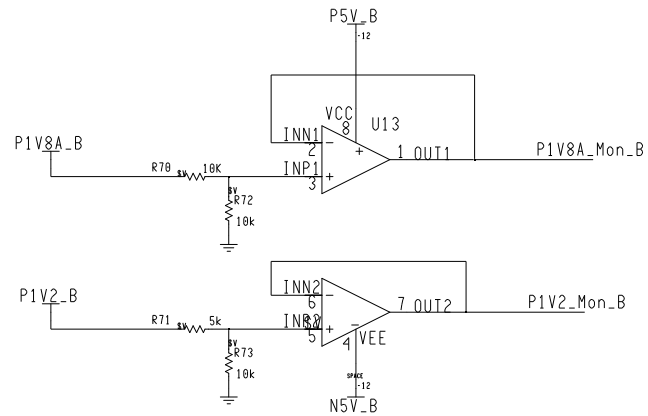
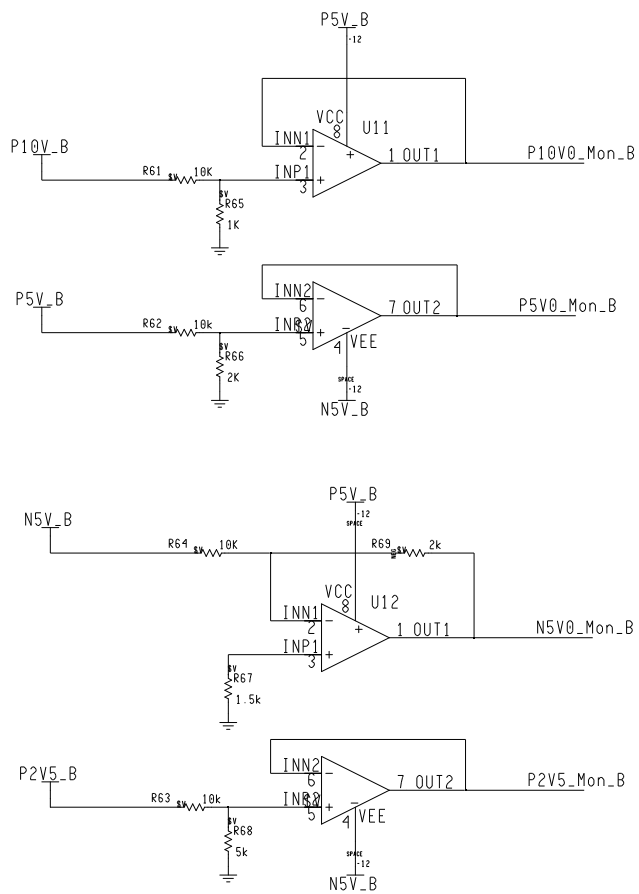
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TITLE
SECTION-A: LV MONITORS

SCH#: B-2799
SPC#: B-2800
ASM#: B-2801

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 ASMH: B-2801

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