## **Quality Control for the 3-in-1 Cards**

## **<u>1. Overview</u>**

The quality control is divided into two phases. The first is a series of acceptance tests done on the cards during manufacturing, to ensure that the production is proceeding as planned. The second phase consists of burn-in and detailed testing of each card before delivery to the PMT-block assembly sites.

## 2. Acceptance Tests

It is proposed that the production rate be limited to 1000 cards/week to allow opportunity for monitoring the production quality. This is stipulated in the instructions to the vendor.

Once production is ready to begin, a group of 30 cards will be prepared by the manufacturer and tested at the University of Chicago. Production will be placed in a hold status until these tests are complete and satisfactory. This step will require the fully-assembled cards to be at Chicago for 2 days.

Once production resumes, a set of 2 cards will be removed from the production stream every hour and sent to Chicago on a daily basis for testing. The results should be available after one day in Chicago. Manufacturing flaws will require production to be halted until any error is corrected.

## **3. Detailed Testing**

A system of 5 Mother Board sets will be used for production testing of the 3-in-1 Cards. This corresponds to a batch of 240 cards. To prepare the batch, all cards will all be visually inspected for manufacturing flaws and a bar-code label applied to each. They will then be connected to a fully functional Mother Board assembly equipped with digitizers for each channel. The set of detailed tests described below will be run on all the cards and any faulty ones removed. The cards will then be burned in at an elevated temperature for 1 week and the tests repeated.

The following tests will be performed on each card:

- 1. Verify the write/read capability of all registers and the proper functioning of all bits.
  - § Reject on any failure
- 2. Measure noise and linearity of high gain and low gain branches using the charge injection system.
  - S High-gain noise from the 3-in-1 card < 2 counts RMS

- S Low-gain noise from the 3-in-1 card < 2 counts RMS
- § High-gain differential non-linearity < 1% (10 counts)
- § Low-gain differential non-linearity < 1% (10 counts)
- § Absolute gain of low-gain branch 1.00 V / 800 pC  $\pm$  10%
- § Gain ratio 64:1  $\pm$  5%
- § Overshoot/undershoot of pulse tail < 5% of peak amplitude for t > 75 ns after peak
- 3. Test integrator functionality using charge injection system
  - S Confirm operation of gate to integrator bus (open and closed)
  - § Gain for each of 6 settings within 10% of nominal
  - § Differential non-linearity < 1% (10 counts)
- 4. Test trigger output functionality using charge injection system
  - S Noise level from 3-in-1 card < 2 counts RMS
  - § Full scale signal within 10% of nominal
  - § Differential non-linearity < 10 counts (1%)
  - S Circuit gating functioning properly when opened and closed
- 5. Test results to be logged with serial number of card, date of test, name of operator.