B2310 V3.1B PCB Specifications

1. Board Layers: 8
2. Layer stack order:
   - Layer1 (File1): Top component layer (Signal_1)
   - Layer2 (File2): Power plane (VCC)
   - Layer3 (File3): Power plane (VCC), (2oz copper)
   - Layer4 (File4): Power plane (GROUND), (2oz copper)
   - Layer5 (File5): Inner signal layer (Signal_2)
   - Layer6 (File6): Inner signal layer (Signal_4)
   - Layer7 (File7): Power plane (VEE)
   - Layer8 (File8): Bottom component layer (Signal_2)
3. Apply solder mask over bare copper on both side:
   - File9: Top solder mask (solder_mask_1)
   - File10: Bottom solder mask (solder_mask_2)
4. Apply silkscreen on both side:
   - File11: Top silkscreen (Silkscreen_1)
   - File12: Bottom silkscreen (Silkscreen_2)
5. Material: FR4 with Tg 170C
6. Board thickness: 0.062'' +/- 0.010''
7. All layers are equal thickness.
8. Layer2 (VCC) and Layer4 (GROUND) use 2oz copper before plating,
   other layers use 1oz copper before plating.
9. All dimensions are in inches unless otherwise noted.
10. PCB fabrication meets IPC-6012: Class 2
11. Box and Twist: Not exceed 0.75%, Test methods meet IPC-TM-650, L=100nm
12. Contact person:
    Fukun Tang
    The University of Chicago
    Tel: 773-702-7801
    Fax: 773-702-2971

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BOARD's DRILL SCHEDULE (Inch)

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<th>DRILL SIZE</th>
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UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

SCH# B2309 V3.1B
SPEC# B2310 V3.1B
ASSM# B2311 V3.1B

SHEET 1 OF 1
DATE 9-20-2000
DRAWN TANG
REV 3.1B