B2428(V3.1B) Board Size (mm)

68.0±.2 (mm)

74.0±.2 (mm)

BOARD SPECIFICATIONS

1. Board Layers: 8

2. Layer Stack Order:
   - Layer1 (Film1): Top component layer(Signal_1).
   - Layer2 (Film2): Power plane(Power,VCC).
   - Layer3 (Film3): Power plane(GROUND).
   - Layer4 (Film4): Inner signal layer(Signal_3).
   - Layer5 (Film5): Inner signal layer(Signal_4).
   - Layer6 (Film6): Power plane(AVCC).
   - Layer7 (Film7): Power plane(AGND).
   - Layer8 (Film8): Bottom component layer(Signal_2).

3. Apply solder mask over bare copper on both side:
   - Film9: Top solder mask.
   - Film10: Bottom solder mask.

4. Apply silk screen on both side:
   - Film11: Top silk screen.
   - Film12: Bottom silk screen.


6. Board thickness: 0.062′′ ±0.010.

7. All layers are equal thickness.

8. Copper thickness test before plating.

9. Ni/Au (Chem plated) over bare copper.

10. All layers minimum trace width/clearance 0.005'/0.006'.

11. All dimensions are in inches unless otherwise noted.

BOARD'S DRILL SCHEDULE (inch)

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Contact person:
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Electronics Development Group
University of Chicago
Tel: (773)-702-7801, Fax: (773)-702-9271

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

B2428 Specification Drawing

TITLE: B2428 Specification Drawing

SCH# 2428V3.1B
SPEC# 2428V3.1B
ASSNY 2428V3.1B

SHEET 1 OF 1
DATE 2/26/2001
DRAWN TANG
REV 3.1B