SEE Tests of the TileCal Optical Interface Board

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1. Overview of Board

This board is located near the center of a 3-m-long TileCal electronics drawer. For events accepted by the Level 1 trigger it receives digital data from the drawer's eight digitizer boards. The data for each event are assembled, formatted and sent out of the drawer on an optical fiber to the TileCal readout driver (ROD) system. In addition, the optical timing trigger and control (TTC) signal is received on this board, converted to electrical form, and distributed to the digitizers and mother board control system in the drawer.

To reduce the probability of losing the data of an entire drawer through the failure of a single component, all systems are duplicated. The input digital signals are distributed to two PLDs for event assembly and formatting. The output of each PLD is sent through separate GLINK transmitters and optical links. Similarly there are two TTC optical receivers. Logic in the PLDs chooses one of the signals for use in the rest of the drawer.

The TileCal system contains 256 such boards; 128 in the barrel and 128 in the extended barrel. The boards can be serviced or exchanged when the electronics drawer is opened during a detector access period.

2. Radiation Requirements

In the TileCal barrel the boards are located at z = 160 cm. and r = 410 cm. Table 1 gives the simulated radiation levels of 21 July 2000, the required safety factors, and resulting radiation tolerance criteria. Radiation levels in the extended barrels are similar or smaller.

Radiation Type	Simulated Level	Safety Factors				Required Level
		Simuln.	Low Dose Rate	Lot Varn.	Total	
Total Ionizing Dose (TID)	0.023 Krad	3.5	5	4	70	1.6 Krad
Non-ionizing energy loss (NIEL)	1.5×10^{10} n/cm^2	5	1	4	20	3.0×10^{11} n/cm^2
Hadrons above 20 MeV (SEE)	6.3×10^{8} h/cm^2	5	1	4	20	1.3×10^{10} h/cm^2

Table 1: Radiation levels for 10 years of 10^7 seconds each, at design luminosity.

3. Test Setup

The tests were performed on 15 September, 2001 at the Indian University cyclotron using 200–MeV protons with their radiation test facility. For these studies the typical flux was 5.8×10^6 p/cm^2/sec and the total fluence per run 2.0×10^{10} p/cm^2, measured with an accuracy of a few percent. Two beam sizes were used. One with a diameter of 6.4 cm was used to irradiate a large portion of the PCB at once, while the second with a diameter of 2.5 cm irradiated individual

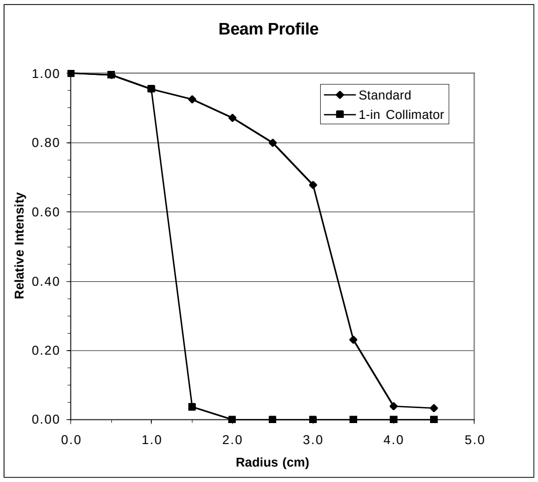

Figure 1: Proton beam profile.

parts. The beam profiles are shown in Fig. 1. It should be noted that a fluence of 2.0×10^{10} 200-MeV protons/cm^2 deposits a total ionizing dose of 1.2 Krad which is 75% of the required level.

The position of the beam on the PCB was determined during the set up process for each run by using a laser directed along the proton beam axis. It was accurate to a millimeter.

As discussed below, data were collected in nine separate runs with the beam size or beam position changed between most runs.

Only one interface board was used for the tests but the design uses multiple copies of many parts. A tally of the number of samples of each part tested appears below.

During the tests the board was fully operational. It received input from eight digitizers boards and transferred data to a CES RIO2 VME processor via an ODIN SLINK destination card. A fixed data pattern from the digitizers was used for each event and the pattern was tested by the on-line computer to ensure integrity. To check for latch-up the power supply current was monitored with a resolution of 5 mA.

3. Run Conditions

The position of the proton beam for each of the nine runs is shown in Figures 2 and 3.

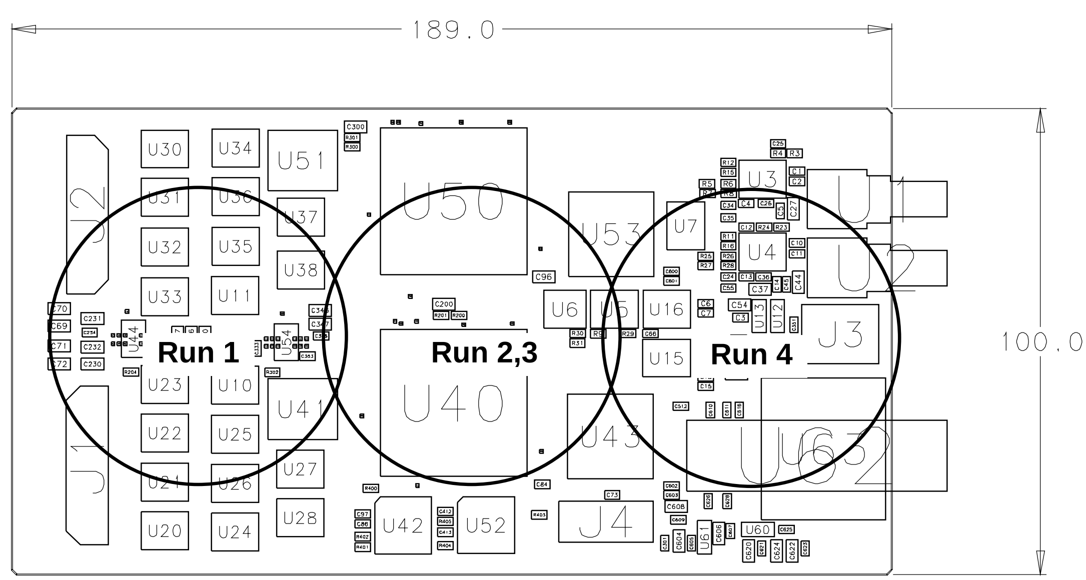

Figure 2: Position of the large beam on the PCB.

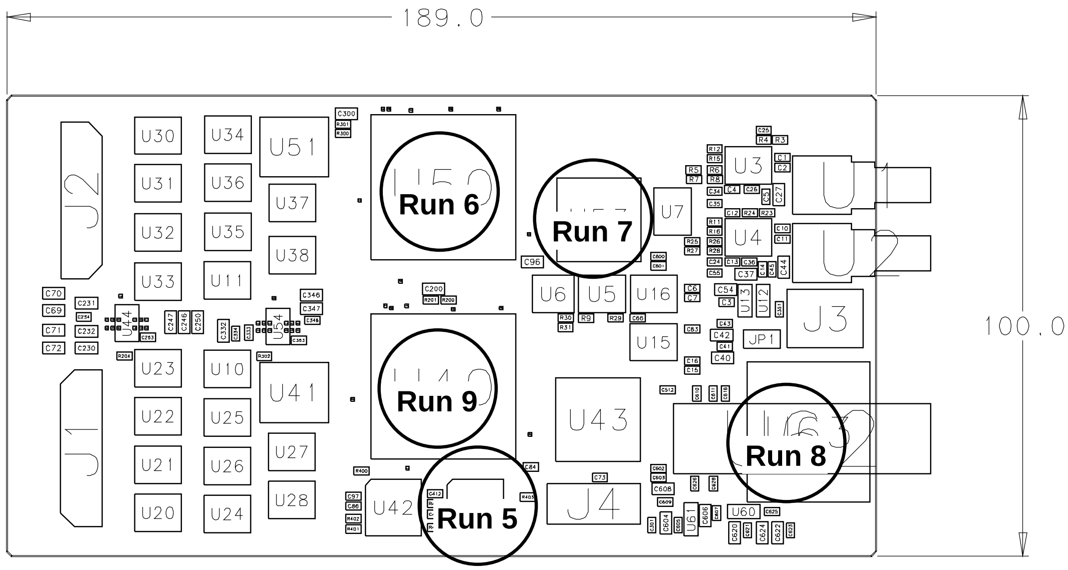

Figure 3: Position of the small beam on the PCB.

Table 2 provides a summary of the data collected for the nine runs together with the number of power resets required. Table 3 gives the detailed specification of the parts.

Run Number	**Components Irradiated**		**Fluence** (p/cm^2)	**Power Reset Errors**
	Ref. Des.	**Function**		
1	U22,U23,U25 U10 U44, U54 U41	LVDS receiver LVDS transmitter 1.8V regulator Clock generator	2×10^{10}	1
2+3	U40 U6	Altera PLD Quad NOR	2×10^{10}	4
4	U2 U4 U7 U15, U16	Optical receiver Post amplifier LVDS transmitter LVDS receiver	2×10^{10}	7
5	U52	Flash memory	2×10^{10}	0
6	U50	Altera PLD	2×10^{10}	2
7	U53	GLINK transmitter	2×10^{10}	0
8	U63	Optical transmitter	2×10^{10}	1
9	U40	Altera PLD	2×10^{10}	1

Table 2: Parts irradiated in each run, the associated fluence, and the number of errors requiring power reset.

Ref. Designation	Part Number	Function	Manuf.
U1, U2	HFBR-2316T	Optical receiver	Agilent
U3, U4	SA5225D	Post amplifier	Philips
U5, U15, U16 U20-U28 U30-U38	DS90LV032ATM	Quad LVDS receiver	National
U6	MC74ACT32D	Quad NOR	ON Semi.
U7, U10, U11	DS90LV031ATM	Quad LVDS transmitter	National
U12, U13, U60, U61	ELJ-RE15NJF2	Inductive power filter	Panasonic
U40, U50	EP20K100QC208	Altera PLD	Altera
U41, U51	SM1100TEV-40.000MHz	Clock generator	Pletronics
U42, U52	EPC2LC20	Flash memory	Altera
U43, U53	HDMP-1032	GLINK transmitter	Agilent
U44, U54	MAX8869	1.8V voltage regulator	Maxim
U63	Custom sub-assembly, Academica Sinica, Taiwan	Dual optical transmitter	

Table 3: Full list of parts and reference designations.

In run 5 the flash memory used to program the PLD was irradiated. The run was paused at the 25%, 50%, 75% and 100% points and the PLD reloaded. Successful operation was restored each time.

4. Results

No destructive failures occurred for any component. The components exposed, the fluence, and the quantity tested are given in Table 4.

Components Irradiated		Fluence	Quantity
Part Number	**Function**	(p/cm^2)	**Tested**
DS90LV032ATM	LVDS receiver	2×10^{10}	5
DS90LV031ATM	LVDS transmitter	2×10^{10}	2
MAX8869	1.8V regulator	2×10^{10}	2
SM1100TEV	Clock generator	2×10^{10}	1
EP20K100QC208	Altera PLD	4×10^{10}	2
MC74ACT32D	Quad NOR	2×10^{10}	1
HFBR-2316T	Optical receiver	2×10^{10}	1
SA5225D	Post amplifier	2×10^{10}	1
EPC2LC20	Flash memory	2×10^{10}	1
HDMP-1032	GLINK transmitter	2×10^{10}	1
Custom	Optical transmitter	2×10^{10}	2

Table 4: Summary of parts tested.

Three types of non-destructive errors were observed. The first were transient errors in the data stream. The second involved permanent errors in the data stream and required a reset of the Altera PLD which was accomplished by cycling the power. The third was a latch-up in which the power supply current was observed to increase by about 60 mA. These were also cleared by power cycling and never resulted in a destructive failure. Because some errors in the data stream caused the DAQ program to hang, the errors can not easily be divided into the three classes. However, the total number of errors which required power cycling were properly counted and their sum is reported in Table 2. From an operational viewpoint this is the important figure. It should be noted that not all of them involve true latch-up.

To evaluate the impact of the necessary power resets on the operation of the TileCal electronics we use the fact that the overall system contains 256 boards in approximately the same radiation environment. Table 2 indicates that 12 reset cases were observed in runs 1 through 4 which covered much of the board with a fluence of 2.0×10^{10} p/cm^2. Given the expected fluence for 10 years reported in Table 1, this number translates to 3.7 power resets per week in one of the 256 electronics drawers. This figure includes the overall safety factor of 20. Such a rate of resets is judged to be entirely acceptable.

5. Further Tests Planned

The board tested was version V3.1 while the production version is expected to be V3.2. The principal difference is that V3.1 uses +5V for the commercial TTC optical receiver and its associated post amplifier, while version V3.2 is designed with a +3.3V optical receiver and amplifiers to eliminate the need for a digital +5V supply. It also uses a larger capacity Altera PLD, of the same series, to facilitate CRC checking. It is planned to repeat the tests described here on several V3.2 boards, as well as to perform TID and NIEL tests as soon as pre-production quantities are available.

5. Conclusions

The SEE tests reported here indicate that approximately 3.7 power resets per week would be needed in one of the 256 TileCal electronics drawers. This estimate is based on the expected hadron fluence augmented by the required safety factor of 20. Further testing with several copies of the production version of the board is required to confirm this result as well as to increase the number of components tested.

Tests of TID and NIEL must also be performed to the required levels and with the necessary number of samples. It is already encouraging that the board has operated successfully with a TID of 1.2 Krad induced by the 200 MeV protons. This represents 75% of the required test level.