B2468V33 PCB STACKUP

Fukun Tang
University of Chicago
Tel:773-702-7801
Fax:773-702-2971
tang@mentor.uchicago.edu

File Name: 2468v33stackup.xls, 2468v33stackup.pdf

12 Layers PCB Stackup

Layer	Artwork	Layer Name	Material Type	Dielectric Thickness (mils)	Trace Width (mils)	Cu Thickness (mils)	Dielectric Constant	Controlled Impedance (Ohms)	Description
1	artwork_1	Top, Signal_1	Conductive		7	0.7		51	Microstrip
			Dielectric	5			4.7		Core/Pre-preg
2	artwork_2	VCC25A	Conductive			1.4			Plane
			Dielectric	8			4.7		Core/Pre-preg
3	artwork_3	Inner, Signal_2	Conductive		7	0.7		50	Unbalanced Stripline
			Dielectric	5			4.7		Core/Pre-preg
4	artwork_4	Inner, Signal_3	Conductive		7	0.7		50	Unbalanced Stripline
			Dielectric	8			4.7		Core/Pre-preg
5	artwork_5	VDD	Conductive			1.4			Plane
			Dielectric	5			4.7		Core/Pre-preg
6	artwork_6	GROUND	Conductive			1.4			Plane
			Dielectric	5			4.7		Core/Pre-preg
7	Artwork_7	AGNDA, AGNDB	Conductive			1.4			Plane
			Dielectric	5			4.7		Core/Pre-preg
8	Artwork_8	VCC30A, VCC30B	Conductive			1.4			Plane
			Dielectric	8			4.7		Core/Pre-preg
9	artwork_9	Inner, Signal_4	Conductive		7	0.7		50	Unbalanced Stripline
			Dielectric	5			4.7		Core/Pre-preg
10	artwork_10	Inner, Signal_5	Conductive		7	0.7		50	Unbalanced Stripline
			Dielectric	8			4.7		Core/Pre-preg
11	artwork_11	VCC25B	Conductive			1.4			Plane
			Dielectric	5					Core/Pre-preg
12	artwork_12	Bot, Signal_6	Conductive		7	0.7	4.7	51	Microstrip

Notes: Total board thickness: 0.070 +/- 0.01 mils
Cotrolled impedence is 50 ohms +/- 10%