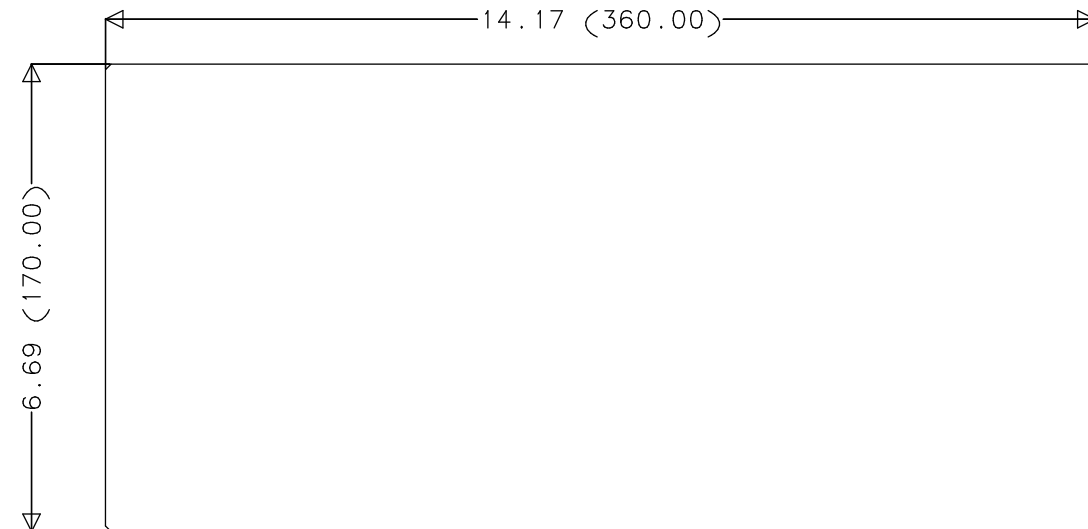


A-2920 Board Size Unit: Inch (mm)



BOARD's DRILL SCHEDULE (Inch)

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.008	588	YES	---
⊞	.01	324	YES	---
⊘	.02	22	YES	---
⊞	.035	240	YES	---
⊘	.041	212	YES	---
⊞	.073	4	YES	---
⊘	.1181	1	YES	---
□	.1378	6	YES	---

Contact person:
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Electronics Development Group
University of Chicago
Tel: (773)-834-4286, Fax: (773)-702-2971

BOARD SPECIFICATIONS

- Board Layers: 10
- Layer Stack Order:
 - Layer1/Artwork_1: Top Signal Layer (signal_1) (0.5 oz)
 - Layer2/Artwork_2: Ground Layer, (0.5 oz)
 - Layer3/Artwork_3: P1V2, Power_2, (0.5 oz)
 - Layer4/Artwork_4: Inner_signal_3 (0.5 oz)
 - Layer5/Artwork_5: Inner_signal_4 (0.5oz)
 - Layer6/Artwork_6: P2V5, Power_3, 0.5 oz.
 - Layer7/Artwork_7: Inner_signal_5 (0.5oz)
 - Layer8/Artwork_8: Inner_signal_6 (0.5oz)
 - Layer9/Artwork_9: P3V3, Power_4, (0.5 oz)
 - Layer10/Artwork_10: Bottom Signal Layer(Signal_2) (0.5 oz)
- Apply silkscreen on both side:
 - Artwork_7: Top silkscreen.
 - Artwork_8: Bottom silkscreen
- Apply solder mask over bare copper on both side:
 - Artwork_9: Top solder mask
 - Artwork_10: Bottom solde mask
- Material: FR4
- Board thickness: 0.072'' +/- 0.010.
- TRACE IMPEDENCE: 50 ohms +/- 10%.
- Copper thickness 0.5oz before plating for all layers.
- Immersion gold plating (3 to 8 micro-inches soft gold) over bare copper
- All layers laid out in mininum trace width/clearence 0.005"/0.005"
- All dimensions are in inches unless otherwise noted.

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
A-2920 Specification

SCH# B-2919
SPC# A-2920
ASM# B-2921

SHEET 1 OF 1
DATE 02/03/2020
DRAWN TANG

B- 2920
REV 1.0